A Negative Capacitance Partially Junction-less Bulk MOSFET with Hysteresis Free Behavior and Improved Performance

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Abstract—Despite the use of High-k gate stacks, poor channel electrostatics at short channel lengths has limited the applicability of conventional Bulk MOSFETs. With the use of Ferroelectric materials in the gate stack, enhanced transverse (gate) electric field has the potential to enable greater scalability, which needs to be further explored in the context of planar Bulk MOSFETs. In this paper, we firstly present the design of an optimized N-channel Partially Junction-less Bulk MOSFET with a view to suppressing various leakage mechanisms, while also taking channel quantization effects into account. Through detailed process simulations, the process steps required to achieve this device design are determined, thus providing a more practical appraisal of the feasibility of the device. We then identify the thickness of the Ferroelectric layer over the existing gate stack with a view to achieve steep sub-threshold slope (SS) while simultaneously ensuring hysteresis-free characteristics, including enhanced Analog as well as Digital performance of the device.

Index Terms—Junction-less MOSFET (JL-MOSFET), Bulk MOSFET, Band-to-Band Tunneling, Metal-Ferroelectric-Insulator-Semiconductor, Sub-threshold Slope (SS), Hysteresis-free, Transconductance Efficiency

I. INTRODUCTION

Increasing demand for smaller, faster circuits consuming lesser power has driven the need for scaling of transistors. In the context of Bulk MOSFETs, this has required aggressive reduction of the oxide thickness (t_{ox}), Source/Drain junction depth (X_j) as well as increasing the doping (Substrate) while also requiring lower power-supply voltages. A key limiting factor in this has been significant gate leakage seen in the dielectrics below 1 nm thickness [1]. With the enhanced lateral electric field, increasing surface DIBL (Drain induced barrier lowering) effects have been seen, thus impacting the ON-State current at the channel located close to the Si/SiO_2 interface (Surface), while also adversely impacting the region away from the Surface, where the gate's control is progressively diminishing resulting in significantly high sub-surface leakage current [2] and hence higher OFF-State current. This leakage current underneath the Si/SiO_2 interface (Sub-surface Leakage) [3] as well as Punch through (both at surface and bulk) [4] [5] and Band-to-Band Tunneling (BTBT) [6] due to band overlap in channel-drain junction, significantly contribute to Static Power Leakage, particularly at shorter channel lengths. These leakage mechanisms need to be mitigated so that transistor scaling continues to provide benefits to circuit designers.

One of the key approaches discussed in literature to obtain good channel electrostatics has been the aggressive reduction of the Effective Oxide Thickness (EOT), thus enhancing the transverse electric field through the use of a High-k material in the gate stack. Due to being thermodynamically stable compared to other High-k dielectrics [7], HfO_2 has emerged as one of the leading candidates to be used as a High-k material in gate stack. In order to obtain improved device performance at shorter channel lengths, it is important to scale the Effective Oxide thickness (EOT) to less than 1 nm, which is possible through scaling of a High-K gate stack comprising of a High-K gate oxide, such as HfO_2 , and the SiO_2 layer below it. However, even with an EOT of less than 1 nm, the improvement realistically achievable both in terms of electrostatics and drive current becomes limited particularly because of channel quantization effects seen in the inversion layer close to the Si/SiO_2 interface [8]. Given these well-documented difficulties in scaling of Bulk MOSFETs, other alternatives to Bulk MOSFETs such as FINFETs and FDSOI structures have been explored, even though these transistors are more complex and more expensive to fabricate [9].

Also, FINFETs have been found to have high parasitic capacitance when compared to bulk MOSFETs [10][11] making them inappropriate for RF applications [12], while also suffering from high parasitic Source/Drain resistance [9]. On the other hand, even though FDSOI structures offer better channel electrostatics compared to conventional bulk MOSFETs through a slight modification in the bulk MOSFET channel doping, device designers have been able to achieve performance identical to FDSOI MOSFETs [13] [9]. Therefore, given simple and well understood fabrication techniques, Bulk MOSFETs can re-emerge as an important device architecture for various applications, provided they can demonstrate good channel electrostatics.

The insufficiency of the High-K gate stack also manifests in the inability of these gate stacks to help transistors achieve sub-threshold slopes steeper than 60 mV/dec at room temperature. This has prompted researchers to look at the possibility of using ferroelectric materials in the gate stack [14], particularly for digital circuit applications. Such transistors termed as negative-capacitance field-effect transistors (NC-FETs) have a gate stack with a ferroelectric material of a suitable thickness deposited on top of an existing gate oxide of a MOSFET, such that the negative capacitance behaviour of the ferroelectric layer added over an existing positive capacitance from the MOSFET device will result in an overall increase in the

gate capacitance. The implication of having a series of one negative and one positive capacitance induces an amplified effect of externally applied gate voltage at the inner interface of the ferroelectric layer and shows negative Drain induced barrier lowering (DIBL), also termed as Drain induced barrier raise (DIBR), with an increase in drain to source voltage, which allows us to further scale the transistors [15]. The enhanced effect of gate voltage inside the channel is likely to curb the degrading effects of drain voltage on the channel electrostatics at shorter channel lengths, making it extremely important to re-explore the Bulk MOSFETs with the inclusion of a Ferroelectric material in the gate stack.

With a large number of leakage mechanisms, such as Sub-surface leakage, BTBT (Band-to-Band tunneling) which primarily impact OFF-state leakage currents, while p-n junction leakage and oxide tunneling impact both ON as well as OFF state currents, at short channel lengths [16][17], a critical first step is to propose a Bulk MOSFET structure with a view to minimizing these leakage phenomena. With an optimized and improved Bulk MOSFET structure, demonstrating lower leakage currents and better electrostatics, the inclusion of a Ferroelectric material in the gate stack is likely to further enhance the device performance and could be a key enabler in scaling of Bulk MOSFETs.

Through TCAD simulations [18], a region of approximately within 2 nm from the surface is identified to be very strongly under the control of the gate, thus significantly contributing to the ON-state current. On the other hand, in a region of approximately within 5 nm from the surface, where the gate has progressively receding influence, weak inversion/sub-threshold current flows. Below this region (within the source/drain junction depth), the gate has negligible influence, thus enabling the sub-surface leakage current, which contributes to the OFF-state current, to flow through this region. Given the importance of different regions in the channel, in terms of their relative contributions to ON-state and OFF-state behaviour of the device, we propose to use the Junction-less architecture as an alternative to obtain higher ON-State currents. Therefore, a key requirement in the design of a Bulk MOSFET is the enhancement of the ON-state current, with a reduction in the OFF-state current. Given the many advantages of Junction-less transistors such as low electric field during ON-state of the device, reduced fabrication complexity because of the absence of a p-n junction, mobility enhancement due to bulk conduction [19], this architecture may be used to enhance the ON-state current. An important challenge to overcome is likely to be large threshold voltage variation [20] with channel thickness compared to bulk MOSFETs [21]. Also, the requirement of heavy doping to get high drive current during ON-state in junction-less transistors, leads to high leakage in OFF-state due to BTBT [6], which is where the lateral doping profile along the source, channel and drain in the Junction-less region becomes important.

In this work, by utilizing the merits of Junction-less (JL) MOSFETs, we propose a partially junction-less MOSFET with high inversion current by having junction-less behaviour close to the surface and a heavily doped (P-type) region closer to the source/drain junction depth to cut down the

sub-surface leakage. Further by determining suitable process steps, we examine the feasibility of the proposed device. In the next step towards further improving the device characteristics, we analyze the performance of the proposed MOSFET by including a ferroelectric layer over the existing High-k gate stack where we show that significant improvement in device performance characteristics such as sub-threshold slope and transconductance efficiency can be obtained in the optimized device without requiring significant scaling of the source/drain junction depth thus providing an incentive to re-examine Bulk MOSFET structures for different applications.

This paper is organized into six sections. In the second section, the proposed partially junction-less Bulk MOSFET structure is discussed, with the TCAD simulation methodology used for simulating the device described in the third section. In the fourth section, we discuss the feasibility of the proposed device by using detailed Process simulations and show that the transfer characteristics of the process simulated device closely emulate the proposed device. Finally, in the fifth section, we show the improvement in device performance that can be obtained by using a Ferroelectric material in the gate stack and we present the conclusion in the sixth section.

Fig. 1: Schematic of Bulk MOSFET depicting the different current carrying mechanisms for $X_j = 30nm$; I_1 : Strong Inversion Current, I_2 : Current due to BTBT, I_3 : Weak Inversion (Sub-threshold) Current, I_4 : Sub-surface Leakage Current; $I_{ON} = I_1 + I_3 + I_4$, $I_{OFF} = I_2 + I_4$

II. DEVICE STRUCTURE AND AN OPTIMIZATION METHODOLOGY

The schematic for Bulk MOSFET with different leakage currents manifesting at shorter gate lengths, is shown in Fig. 1, in which the electrostatics in a region close to the Si/SiO_2 interface (Surface) is primarily controlled by the electric field from the gate. While on the other hand, the regions away from the surface, with diminishing control from the gate, has a relatively greater control of drain electric field over the channel. Thus, it has been observed that the region through which the strong inversion current flows is extremely narrow (approximately within 2nm from the surface), while the sub-threshold/weak inversion current (I_3) flows over a slightly

wider region, where the influence of the gate voltage though still present, begins to recede. Moreover, the sub-surface leakage current (I_4) flows over a region farther away from the surface, where the gate has negligible influence. In addition, due to tunneling of electrons between the valance band of the channel and the conduction band of the drain, under accumulation bias, the flow of band-to-band tunneling current (I_2) near the surface also becomes significant and needs to be considered. Having identified the prominent current carrying mechanisms including leakage mechanisms that are likely to manifest in short-channel Bulk MOSFETs, it becomes important to suitably design these MOSFETs with a view to enhancing the ON-state current while simultaneously reducing the OFF-state current, so as to improve the device switching characteristics.

We therefore propose an optimized partially junction-less bulk MOSFET structure, as shown in Fig. 2, for a gate length of 10 nm. The device includes a P-type substrate ($N_{sub} = 10^{18} \text{cm}^{-3}$) and a thin N-type layer of 3 nm thickness close to the Si/SiO_2 interface, making the device junction-less at the surface, where the doping in the channel ($N_{channel_1} = 10^{19} \text{cm}^{-3}$) is higher than the doping in the source ($N_{source_1} = 5 \times 10^{18} \text{cm}^{-3}$) and drain ($N_{drain_1} = 10^{17} \text{cm}^{-3}$) regions, thus enhancing the drive current capability of the device. High doping in the channel at the surface compared to the drain ensures a wider depletion region in the drain side compared to the channel thus lowering the possibility of DIBL and BTBT, while a slightly higher doping of the source compared to the drain at the surface enables obtaining a higher ON-state current. A narrow region in the channel below the junction-less region of the thickness of approximately 2 nm, where the gate continues to have an influence, is heavily P-type doped ($N_{channel_2} = 5 \times 10^{18} \text{cm}^{-3}$), while at the source and drain doping corresponding to this region is reduced ($N_{source_2} = N_{drain_2} = 10^{18} \text{cm}^{-3}$) to ensure control of the sub-threshold leakage. The rest of the channel, below the heavily doped P-type region is a region where the gate has relatively no influence and is susceptible to sub-surface leakage current. It is therefore important to have reasonably heavy P-type doping ($N_{channel_3} = 10^{19} \text{cm}^{-3}$) in this region (below Channel_2) so as to reduce the sub-surface leakage on one hand, while ensuring that sub-threshold slope is not adversely impacted, and the threshold voltage is not significantly increased. Through a moderately P-type doped region ($N_{channel_2} = 5 \times 10^{18} \text{cm}^{-3}$) of thickness 2 nm, better control of the sub-threshold slope can be achieved while also enabling a smoother transition from the junction-less channel of heavy N-type doping of a thickness of 3 nm to the heavily P-type doped region closer to the source/drain junction depth.

Careful identification of the regions where the ON-state current and sub-threshold current is likely to flow, closer to the Si/SiO_2 interface, enables optimization of these currents through suitable channel doping. Also the reduction of the undesired sub-surface leakage current through a combination of relatively higher P-type doping in the channel and lower N-type doping in the source and drain, makes it more practical to have a deeper source and drain junction ($X_j = 30 \text{nm}$). Besides optimizing the source, drain and channel doping,

Fig. 2: Schematic of the proposed optimized partially junction-less Bulk MOSFET, where $X_j = 30 \text{nm}$, $t_{\text{HfO}_2} = 1 \text{nm}$, $t_{\text{SiO}_2} = 0.7 \text{nm}$

another critical aspect in enhancing channel electrostatics involves increasing the effects of the electric field from the gate through the use of a practical High-k gate stack with an EOT of 0.88 nm ($t_{\text{HfO}_2} = 1 \text{nm}$ and $t_{\text{SiO}_2} = 0.7 \text{nm}$) [22].

III. SIMULATION METHODOLOGY

For all the device simulations Synopsys TCAD device simulator [18] is used. Poisson's equation for both electrons and holes is solved self-consistently with Drift-Diffusion and Continuity equation, which is widely used for shorter channel Bulk MOSFETs [23]. For considering the effect of heavy doping on the band gap, a band gap narrowing model is used, while the leakage due to p-n junctions is considered through a Shockley-Read-Hall recombination model. For tunneling at the Drain-channel junction, Non-local Band-to-Band tunneling model is considered. The high field dependence of the carriers inside the channel is considered through the Philips mobility model. In addition to that, the effect of channel quantization is considered through the use of the QC Vandort Model. Furthermore, through the inclusion of the Landau-Khalatnikov equation, along the direction perpendicular to the direction of carrier transport, in the self-consistent Poisson's equation solution, the effect of using the Ferroelectric in the gate stack on the channel electrostatics is effectively taken into account.

IV. FEASIBILITY OF THE PROPOSED PARTIALLY JUNCTION-LESS BULK MOSFET: A POSSIBLE PROCESS FLOW

In this section, we show a possible process flow, as described in Fig. 3, which is very close to the process flow of Bulk MOSFETs [24]. In the process flow shown in Fig. 3, one of the important steps to ensure that the required gate length can be obtained is through precise masking. This step prevents lateral diffusion of the source/drain dopants into the channel [25]. The doping and junction depth of the source and drain

- Silicon Wafer with Initial Concentration (Boron) of $6 \times 10^{18} \text{ cm}^{-3}$
- Diffusion of carriers at 1050°C for a duration of 1 minute
- Oxidation at 800°C for a duration of 2 minute
- Etch the Oxide in source/drain region through proper masking
- Implant Phosphorus with dose and energy of $2 \times 10^{13} \text{ cm}^{-2}$ and 2 keV respectively in source/drain region
- Use temperature of 950°C for 5 minutes to diffuse the carriers
- Etch Oxide in the gate region precisely to get thickness(t_{SiO_2}) of 0.7 nm
- Implant Phosphorus in the gate region with dose of $8 \times 10^{12} \text{ cm}^{-2}$ and energy of 0.12 keV through proper masking to get an N-type channel close to Si/SiO₂ interface
- Diffuse carrier with temperature 780°C for only 1 Second
- Deposit 1nm thick HfO₂ in the gate region
- Implant Phosphorus with dose $5 \times 10^{11} \text{ cm}^{-2}$ and energy 0.12 keV through precise masking to get source/drain extension region
- Diffuse carrier with temperature 780°C for only 1 Second
- Make Source, Drain, Gate and Substrate contacts

Fig. 3: Process flow for the proposed partially junction-less bulk MOSFET

Fig. 4: Partially junction-less bulk MOSFET simulated using process steps shown in Fig. 3

is controlled through the dose of the Phosphorus dopants, its energy and the initial Boron concentration of the substrate. Similarly, the doping and depth of the N-type junction-less region close to the surface is controlled through the dose rate and implant of the Phosphorus dopants, while precise masking will prevent the channel dopant from diffusing into the source and drain. A very important step is the growth of the source/drain extension whose doping, depth and length is determined by the dose rate, implant energy and masking respectively. The depth of the source/drain extension is vital towards controlling the ON-state current and reducing the weak inversion current, ensuring a steeper sub-threshold slope. In addition through the oxidation time and temperature, the oxide is grown over the source, drain and channel, which through etching can enable the growth of the SiO₂ gate oxide of desired thickness (0.7 nm) over the channel. Finally, the gate stack is completed by depositing a 1 nm HfO₂ layer in the gate region. Through these process steps, the partially junction-less Bulk MOSFET is shown in Fig. 4.

Fig. 5: Comparison of transfer characteristics (Drain Current in log scale versus gate to source voltage) of the proposed partially Junction-less bulk MOSFET (shown in Fig. 2) and process simulated device clearly indicates that the two devices are in close agreement

This MOSFET structure obtained is a feasible representation of the optimized Bulk MOSFET structure shown in Fig. 2. Therefore, through these critical process steps, an N-type junction-less channel of higher doping than the source/drain can be obtained, thus resulting in a higher ON-state current close to the surface while also being able to control the BTBT leakage current under accumulation bias. At the same time the heavily doped Phosphorus implants at the surface will push the Boron implants deeper into the channel, creating a heavily doped P-type region away from the surface, thus effectively controlling both the sub-threshold and sub-surface leakage currents.

Through the device obtained from the process simulation, shown in Fig. 4, the idealized device structure in Fig. 2 is compared to get identical electrostatics parameters (SS, $I_{\text{ON}}/I_{\text{OFF}}$, V_{th} and I_d at $V_{\text{gs}} = -2\text{V}$), where the sensitivity of the electrostatics parameters is thoroughly investigated and presented in the Supplementary material. From this investigation it is observed that the design parameters chosen in Fig.2 are indeed optimum. In Fig. 5, we show the comparison of the transfer characteristics between the process simulated device and the device shown in Fig. 2, where the proposed device has the same threshold voltage as obtained from the process simulated device, while the sub-threshold slope and $I_{\text{ON}}/I_{\text{OFF}}$ ratios are nearly identical for both the devices. Through the very good agreement of the transfer characteristics of the two devices, it may be seen that the electrostatics seen in the devices are nearly identical.

V. INCORPORATION OF A FERROELECTRIC MATERIAL BASED GATE STACK IN THE PROPOSED PARTIALLY JUNCTION-LESS STRUCTURE

In the proposed partially junction-less Bulk MOSFET structure, shown in Fig. 2, further improvement in the transfer characteristics are achieved, through the inclusion of a Ferroelectric in the gate stack. Besides improving the sub-threshold

slope significantly, the inclusion of a Ferroelectric layer of thickness of 4 nm in the gate stack will also eliminate the tunneling current through the gate oxide [6]. The Ferroelectric material has been deposited on the existing High-k gate stack, with the Ferroelectric material parameters reported by Agarwal *et al.*[26] used for the simulation of the electrostatics of the Metal-Ferroelectric-Insulator-Semiconductor (MFIS) FET structure, which is found to be more practical compared to the Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) structure [27]. The use of a Ferroelectric material in the gate stack of a short channel MOSFET has been reported to result in Drain induced barrier raise (DIBR) [28]. The choice of t_{Ferro} (thickness of ferroelectric layer) is based on achieving Hysteresis-free characteristics with minimized DIBR, while keeping the sub-threshold slope independent of drain to source voltage (V_{ds}) variations. With this Metal-Ferroelectric-Insulator gate stack over the proposed device, shown in Fig. 2, we show an improved sub-threshold slope with threshold voltage, in the range of 0.12 V to 0.22 V, for V_{ds} of 50 mV to 0.77 V, respectively. In Fig. 6, we show the comparison of the device transfer characteristics with and without using a layer of ferroelectric material, over the existing gate stack, for a gate length of 10 nm, where the inclusion of the ferroelectric layer over the High-k gate stack improved the sub-threshold slope substantially for both V_{ds} of 50 mV and 0.77 V, while ensuring the Hysteresis-free behavior. At the same time, the Analog performance parameters such as transconductance (g_m) and transconductance efficiency (g_m/I_d), shown in Fig. 7 and Fig. 8 respectively, are found to be superior than the values reported in literature [29] [30].

Fig. 6: Comparison of transfer characteristics (Drain Current in log scale versus gate to source voltage) of the proposed partially Junction-less bulk MOSFET with and without using a ferroelectric material over the high-k gate stack

Similarly, for gate lengths from 14 nm to 30 nm with identical doping as shown in Fig. 2 and 4 nm thick ferroelectric layer inside the gate stack, the observed values of threshold voltage remain 0.12 V and 0.22 V (close to ITRS specifications [31]), at V_{ds} of 50 mV and 0.77 V, respectively, while the values for sub-threshold slope, are shown in table I. This indicates that the threshold voltage of the device is immune to variation in gate length, which is due to the decreasing value

Fig. 7: Transconductance versus Gate to Source Voltage for gate length of 10 nm with a 4 nm ferroelectric layer

Fig. 8: Transconductance Efficiency versus Drain Current for gate length of 10 nm with a 4 nm ferroelectric layer

of DIBR with increasing gate length, as shown in table II, where DIBR is calculated with reference to the value of V_{ds} , beyond which threshold voltage starts to increase with V_{ds} , denoted as (transition drain to source voltage) V_{ds_t} . Also, for $V_{ds} < V_{ds_t}$ zero DIBL is seen. In this paper, we define DIBR as shown in equation 1:

$$DIBR = (V_{th_1} - V_{th_2}) / (V_{dd} - V_{ds_t}) \quad (1)$$

where V_{th_1} is the threshold voltage when $V_{ds} = V_{dd}$ and V_{th_2} is the threshold voltage when $V_{ds} = V_{ds_t}$. In this work, we have shown that through a slight modification of the Bulk MOSFET structure, discussed in this paper, with the inclusion of a thin Ferroelectric layer of thickness of just 4 nm in the gate stack, the undesired influence of the drain on the channel's electrostatics has been significantly reduced, thus enabling the gate length of the Bulk MOSFET structure to be scaled up to 10 nm, while obtaining improved analog and digital device performance.

VI. CONCLUSION

In this work, we propose an optimized partially junction-less bulk MOSFET, with reduced leakage currents, without signifi-

TABLE I: Sub-threshold Slope (SS) for different gate lengths (L_g)

L_g (nm)	SS (mV/dec) ($V_{ds} = 50mV$)	SS (mV/dec) ($V_{ds} = 0.77V$)
10	65	77
14	53	54
17	52	53
20	52	53
30	52	53

TABLE II: Transition Voltage (V_{dst}) and DIBR values for different gate lengths, where $V_{th1} = 0.22$ V, $V_{th2} = 0.12$ V, for all gate lengths considered

L_g (nm)	V_{dst} (V)	V_{dd} (V)	DIBR (mV/V)
10	0.29	0.77	208
14	0.25	0.77	192
17	0.22	0.77	181
20	0.16	0.77	163
30	0.06	0.77	140

cantly scaling source/drain junction depth (X_j) and power supply voltage (V_{dd}). Additionally, through process simulations, a set of possible process steps are outlined to realize the device with a view to matching its transfer characteristics with that of the proposed device. Furthermore, an optimum choice of the Ferroelectric layer over the existing gate stack, enabled us to obtain superior sub-threshold slope along with Hysteresis-free characteristics, good transconductance efficiency and immunity to threshold voltage variation, over a wide range of drain to source voltages (V_{ds}).

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SUPPLEMENTARY MATERIAL

Percentage Variation Study of Doping and thickness of regions in the channel and their effects on the electrostatics parameters.

AUTHOR CONTRIBUTIONS

Harshit Kansal: Conceptualization, Methodology, Data curation, Writing- Original draft preparation, Visualization, Investigation, Writing- Reviewing and Editing. Aditya Sankar Medury: Conceptualization, Methodology, Visualization, Investigation, Supervision, Writing- Reviewing and Editing.

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