Exploiting Drain-Erase Scheme in Ferroelectric FETs for Logic-in-Memory

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Abstract— The conventional computing platforms based on von-Neumann architecture are highly space- and energy-intensive while handling the emerging applications such as AI, ML, and big data. To overcome the von Neumann bottleneck, compact and light-weight logic-in-memory implementations of Boolean logic gates based on emerging non-volatile memory (e-NVM) such as RRAMs, PCM, STT-MRAMs, etc., were proposed recently. However, these e-NVMs not only exhibit significant temporal and spatial variability, but their large-scale integration with CMOS process is also a technological challenge. To overcome these issues with the emerging non-volatile memories, Ferroelectric FETs based on CMOS-compatible doped Hafnium oxide with the capability of large-scale CMOS integration in the advanced logic nodes were proposed. Considering the high scalability and CMOS-compatibility of the FeFETs, in this work, for the first time, we propose a logic-in-memory implementation utilizing a single ferroelectric fully-depleted-silicon-on-insulator (Fe-FDSOI) FET exploiting the unique drain erase phenomenon. In our proposed logic-in-memory implementation, inputs are applied at the gate and drain terminals using a novel input-to-voltage mapping scheme, and output is obtained as the current flowing through the Fe-FDSOI FET. We utilize an experimentally calibrated compact model of the ferroelectric capacitor connected to the baseline industry standard BSIM-IMG compact model for the FDSOI transistor for proof of concept demonstration. We also perform a comprehensive analysis of the performance metrics of the proposed logic-in-memory implementation. Our results indicate that we can realize at least 10 Boolean logic gates with high energy and area-efficiency utilizing the proposed scheme.

Index Terms— Drain-Erase, Ferroelectric FETs, Logic-in-memory, Reconfigurable logic gates.

I. INTRODUCTION

THE unprecedented growth in data generation and processing in this artificial intelligence (AI) and the internet of things (IoT) era has led to a surge in demand for energy-efficient computing primitives [1], [2]. However, handling such computations with the traditional von-Neumann platforms is difficult due to the significantly large energy and latency overhead owing to the enormous data transfer between the memory and processing units [3]–[5]. Therefore, non-von Neumann computing primitives such as neuromorphic computing, in-memory computing, and logic-in-memory implementations

have gained significant attention recently [6]–[8]. Logic-in-memory is a novel technique where the logic operation is performed within the memory device (without data transfer to the processing unit) by leveraging its non-volatility. Logic-in-memory implementations facilitate the compact realization of a Boolean logic gate by reducing the transistor count [9], [10]. Since logic gates form the fundamental element of all computing systems, collocating logic, and memory blocks not only increases the computational speed and throughput but also leads to a significant reduction in energy by eliminating data transfer.

Recently, several emerging non-volatile memories, such as PCM, RRAMs, STT-MRAMs, etc., have been utilized for efficient logic-in-memory implementations. Although PCM is a relatively mature technology and exhibits a high endurance and fast switching speed (~ 100 ns), the large reset current required to heat the phase change material beyond the melting point results in extremely high energy consumption. While RRAMs exhibit high scalability, their limited endurance, high spatial and temporal variations, and sneak path leakage current, when used without a selector device limits their applications. Moreover, the large-scale integration of these emerging non-volatile memories with the CMOS technology is a technological challenge.

FeFETs based on doped hafnium oxide have witnessed a surge in their research and development activities due to their CMOS compatibility, low write latency, high scalability, low program/erase energy, and multi-level storage capability [11]–[13]. Furthermore, FeFETs based on 22 nm and 28 nm technology have already been demonstrated [14], [15]. FeFETs have been demonstrated successfully in neuromorphic computing, hardware security primitives, and also as embedded nonvolatile memory [16]–[18]. Apart from using voltage pulses at the gate terminal for programming/erase operations, recently, in [19], it was shown that the polarization state can also be altered by applying appropriate voltage pulses at the drain terminal of Fe-FDSOI FETs. This drain-erase scheme facilitates the utilization of Ferroelectric FET-based memory cells in a stacked configuration similar to the mature 3D NAND flash memory technology. Furthermore, it was also shown that the memory window can be substantially increased by using an asymmetric double-gate structure in Fe-FDSOI FETs [20], [21].

Moreover, FeFETs were also explored recently for logic-in-memory implementations [22], [23]. NAND and NOR gates were realized within FeFETs in [22] by storing one input as the polarization state and applying the other input during the read process. Moreover, multiple logic gates were implemented in

[23] utilizing both front and back gate bias for programming the FeFETs. However, in a crosspoint array structure where all the cells share the same substrate, programming through the back gate may not be feasible, and applying voltages on the back gate may perturb the existing logic realizations. Also, a three-step approach was utilized in [23], which may limit the speed of logic operations. To realize the true potential of the logic-in-memory primitives, we need a highly reconfigurable fast implementation. Moreover, an energy-efficient and compact run-time reconfigurable logic gate implementation also shows an enhanced immunity against reverse-engineering attacks [24].

Considering the potential benefits of a reconfigurable logic-in-memory implementation from computing and security aspects, in this work, for the first time, we propose a novel Ferroelectric FET-based logic-in-memory implementation utilizing the drain erase scheme. We have designed a novel input-to-voltage mapping scheme for the gate and drain terminals to efficiently exploit the drain erase scheme and obtain the desired logic gate output as the drain current of Fe-FDSOI FET. For proof of concept demonstration and performance benchmarking, we utilize an experimentally calibrated compact model for Fe-FDSOI FETs. Our implementation shows high reconfigurability as ten logic gates can be implemented in a single FeFET with fewer steps, unlike prior approaches [22], [23], which is more than previous FeFETs based implementations while consuming ultra-low energy and a small area, paving the way for performing secured and high-density logic-in-memory operations.

II. METHODOLOGY

The Fe-FDSOI FET utilized in this work for proof of concept demonstration is shown in Fig. 1. It consists of a thin layer of zirconium-doped hafnium oxide in the gate stack. For emulating the Fe-FDSOI FET, we first utilize a circuit-compatible FE capacitor based on a multi-domain Preisach model [25] and tune the model parameters to mimic the measured characteristics [26], as shown in Fig. 2. Furthermore, the Fe-FDSOI model is derived by connecting the calibrated FE cap model to the gate electrode of the industry standard BSIM IMG model [27], [28].

In FeFETs, the polarization state of the ferroelectric layer dictates the threshold voltage of the FeFET. Based on the direction of polarization of the FE layer in the gate stack, FeFET can transition between a low V_{TH} state and a high V_{TH} state by applying an appropriate program and erase pulse on the gate terminal. Generally, low V_{TH} and high V_{TH} states are achieved by applying large positive and negative pulses on the gate terminal, respectively, as shown in Fig. 3(a). The corresponding transfer characteristics of the two states, erase and program, are shown in Fig. 3(b). Since we need to realize logic gates with binary inputs, we have utilized the extreme polarization states and threshold voltages in this work.

Moreover, to utilize FeFETs in 3D NAND architecture for in-memory computing and inference and realize true random access by facilitating program/erase/inhibition of individual cells in NAND array without disturbing the neighbor cells, a
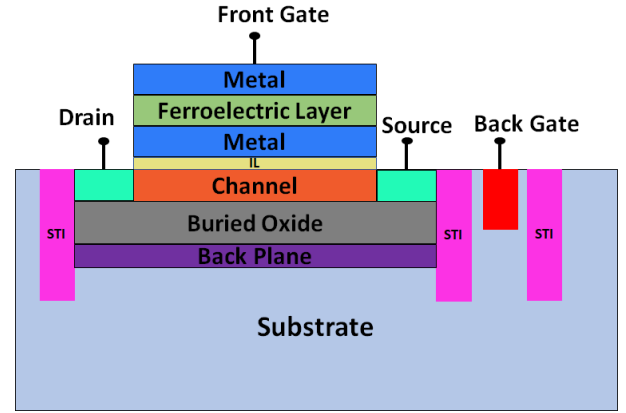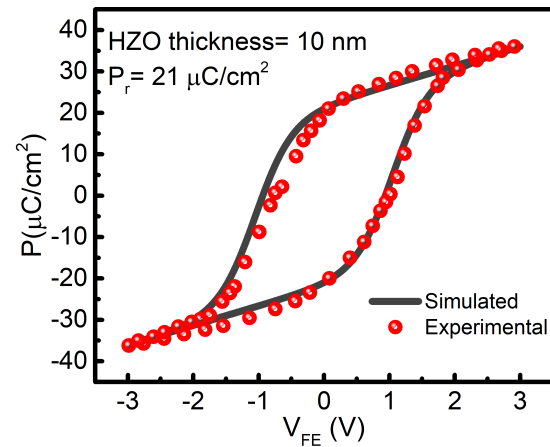

Fig. 1. Schematic of Fe-FDSOI FET used.

Fig. 2. P-V calibration of FeCAP with experimental data [26].

novel drain erase scheme was proposed in [19]. Furthermore, the efficacy of the drain-erase scheme is significantly high in confined channel architectures such as FDSOI due to a larger BTBT (band-to-band tunneling) [29], [30]. The drain-erase scheme also facilitates multi-level capability in the Fe-FDSOI FETs. To illustrate the drain-erase operation, we have shown the pulses applied at the drain, gate, and source terminals in Fig. 4(a). The device is initialized first in the same programming state by applying a large positive voltage pulse on the gate electrode. For inducing multi-level capability through the drain-erase scheme, a voltage pulse of increasing amplitude is applied on the drain terminal in different iterations while the source terminal is kept at 1.5 V to maximize the dynamic range of drain current [19]. After the application of drain-erase pulses, the state of the Fe-FDSOI FET is read by sweeping the voltage from -0.1 V to 0.1 V at the gate terminal while keeping the drain and source electrodes at 0.05 V and 0 V, respectively. The transfer(read) characteristics for different drain erase pulses are shown in Fig. 4(b). As can be seen in Fig. 4(b), the drain current reduces with an increase in the applied pulse amplitude at the drain terminal. For dealing with binary inputs of logic gates in this work, we have used extreme values of the drain-erase pulses.
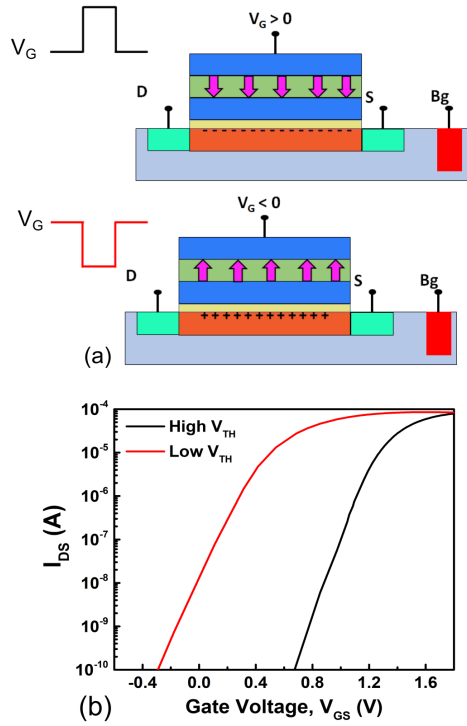
Fig. 3. (a) Tuning of FeFET in two polarization states (b) Transfer characteristics of PRG/ERS states.

Logic Gate	V_g for Input A=0	V_g for Input A=1	V_d for Input B=0	V_d for Input B=1
AND	0 V	5 V	5 V	0 V
INHIB	5 V	0 V	5 V	0 V
N-IMPLY	0 V	5 V	0 V	5 V
NOR	5 V	0 V	0 V	5 V
OR	0 V	5 V	0 V	-5 V
N-INHIB	0 V	5 V	-5 V	0 V
IMPLY	5 V	0 V	0 V	-5 V
NAND	5 V	0 V	-5 V	0 V
NOT	-	-	0 V	5 V
BUFFER	-	-	5 V	0 V

III. LOGIC-IN-MEMORY IMPLEMENTATION

To implement two-input logic-gates utilizing a single Fe-FDSOI FET, we have exploited their ability to modulate the threshold voltage via programming/erasing pulses applied on gate and drain terminals. Furthermore, we propose a novel input-to-voltage pulse mapping scheme that encodes the logic level of the inputs into the voltage pulse amplitude to be applied on the gate and drain terminals for implementing a particular logic gate. Utilizing the novel mapping scheme, multiple logic gates can be implemented within a single Fe-FDSOI FET, giving an additional runtime reconfigurability feature. The input-to-voltage mapping scheme for 10 different logic gates has been listed in Table I. Here, we explain the operation of the universal NOR gate.

The truth table and the symbol of a 2-input NOR gate with inputs A and B, and output C are shown in Fig.5(a). As can be observed from the truth table of a NOR gate, the output at logic level '1' only when both the inputs are at logic level '0', and for all other cases, the output is at logic level '0'. To implement NOR gate using Fe-FDSOI FET, the inputs
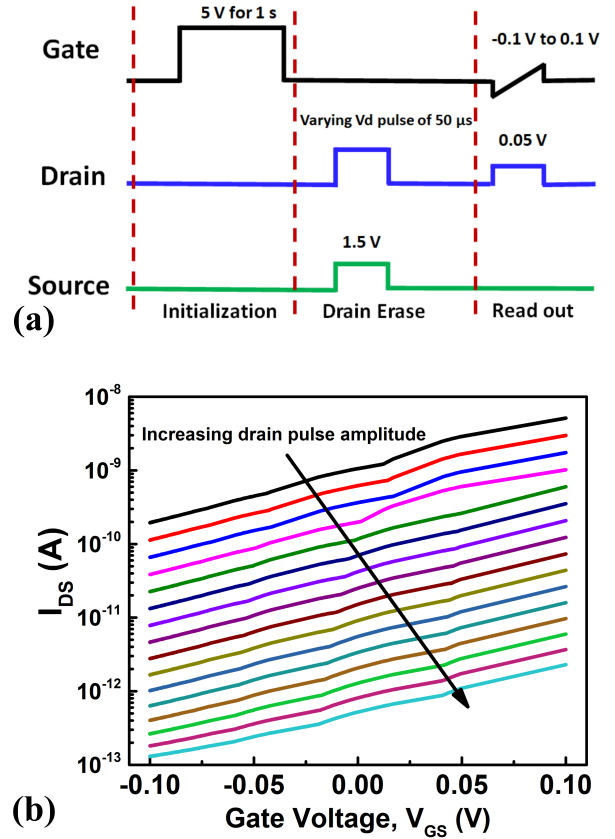

Fig. 4. (a)Drain, Gate, Source voltage waveforms for drain for erase operation (drain voltage in erase operation varied from 2 to 5 V in steps of 0.2 V). (b) Transfer(read) characteristics corresponding to different drain erase voltages.

A and B are applied as gate and drain pulses, respectively. Based on the input combination of gate and drain pulses, the polarization state of the ferroelectric layer within the gate stack may be changed, which ultimately modulates the threshold voltage of the Fe-FDSOI FET. Here, input A is encoded as a logic level '0' by applying a pulse of amplitude 5 V and duration $50\mu s$ at the gate terminal, while logic level '1' is realized by connecting the gate terminal to the ground for the same duration. However, input B, logic level '0' is encoded by connecting the drain terminal to the ground, while logic level '1' is realized by the application of a voltage pulse with an amplitude of 5 V and duration of $50\mu s$ at the drain terminal. FeFET is reset by applying a large negative pulse at the gate while grounding the drain and source. Unlike [23], where different initializations are done for different logic implementations, leading to an additional delay and reduction in the throughput, the conventional reset process is used in this work. The different input combinations and the corresponding voltages applied to the drain and gate terminals are shown in Figs.5 (b)-(e). During the application of inputs, the source is kept at 1.5 V to enhance the effect of drain erase [19]. The output is encoded as the drain current of the Fe-FDSOI FET, and a high drain current (low V_{TH} state) is considered as logic level '1' and a low drain current (high V_{TH} state) is considered as logic level '0'. For reading the output, a gate
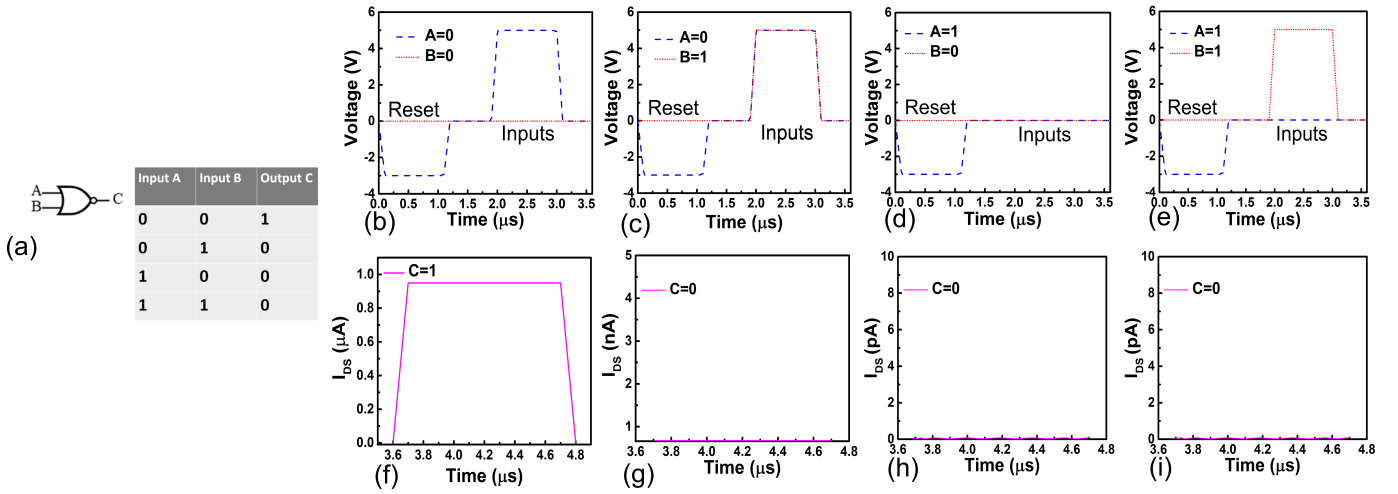
Fig. 5. (a) Symbol and truth table of the NOR gate. Input Voltage waveforms for input combinations (b)00 (c) 01 (d)10 (e)11, their output waveforms are shown in (f)-(i) respectively. A reset operation is performed every time before the application of inputs. Output characteristics are extracted at V_{gs}=0.1 V and V_{ds}=0.05 V
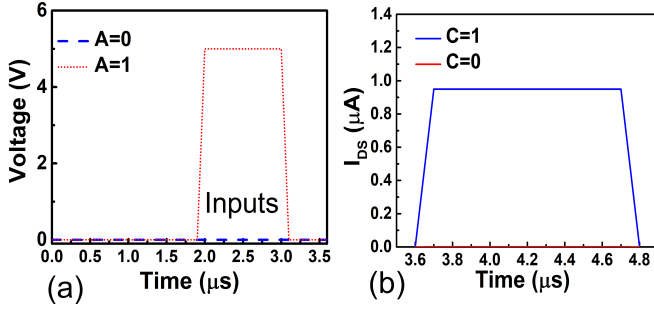

Fig. 6. (a) Input voltage waveform (b) output characteristics of a NOT gate.

voltage of 0.1 V and a drain voltage of 0.05 V are applied while grounding the source and body terminals. The output current characteristics for all the input combinations are shown in Figs.5 (f)-(i). As can be seen in Fig. 5, the output current is considerably high only when both the inputs are at logic level '0', whereas, for all other input combinations, there is almost negligible current.

Similarly, the NOT gate can be implemented by applying a positive programming pulse to the gate and applying a pulse at the drain side based on the input. A 0 V and 5 V pulse at the drain represents logic level '0' and logic level '1', respectively. Connecting the drain terminal to the ground results in the programming of the Fe-FDSOI FET to the low V_{TH} state, whereas application of 5 V at the drain terminal inhibits the programming through the gate terminal, and Fe-FDSOI FET remains in the same initial V_{TH} (polarization) state. The input/output waveforms for the NOT gate are shown in Fig. 6.

IV. PERFORMANCE METRICS

A. Delay

The output delay is defined as the time taken to read the output after application(programming) of the inputs. Due to

parasitic charge trapping, the polarization-state of the ferro-electric FETs state cannot be read immediately after writing. However, by using SiN_x as an interfacial layer which results in the negligible charge trapping [31] and also by applying an appropriate standby bias [32], this delay can be substantially reduced, and the Ferroelectric FETs state can be read immediately(10 ns) after the writing process. In our implementation, the output is read after 500 ns.

B. Area

The proposed logic-in-memory implementation uses only a single Fe-FDSOI FET and occupies an area of 0.07 μm^2. Our implementation utilizes only a single Fe-FDSOI FET and does not require an additional pull-up device as compared to the previous FeFET-based implementation [22], where only NAND/NOR logic was demonstrated using an additional pull-up device. Hence, our proposed implementation implicitly provides scaling benefits.

C. Energy

The proposed logic-in-memory implementation utilizing a single Fe-FDSOI FET takes two steps: (i) Applying voltage pulses at the gate and drain terminals according to the inputs and (ii) reading the state of the Fe-FDSOI FET, as can be seen in Fig. 5. Therefore, energy consideration from both the steps are calculated and are termed as write and read energy. The maximum read and write energy consumed by the proposed implementation are 47.5 fJ and 3.3 nJ, respectively.

V. CONCLUSION

In this work, we have proposed a novel, highly scalable, compact, energy-efficient, and reconfigurable logic-in-memory implementation by exploiting the drain-erase scheme utilizing a single ferroelectric FDSOI FET. Our novel input-to-voltage pulse mapping schemes for the voltages applied to the gate and drain terminals of Fe-FDSOI FET facilitate the realization

of at least ten Boolean logic gates in a single Fe-FDSOI FET, leading to a highly reconfigurable architecture which may be utilized for energy-efficient computing and hardware security. We believe that our work will provide incentive for the experimental realization of compact and energy-efficient logic-in-memory implementations utilizing CMOS-compatible ferroelectric FETs.

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