Bidirectional Isolated DC-DC Converter with High Static Gain: Analysis and Experimentation

Ygor Pereira Marca and Ivo Barbi, *Life Fellow, IEEE*

***Abstract* - A bidirectional isolated DC-DC converter with high efficiency and static gain, formed by the combination of a FB-ZVS-PWM and a current fed push-pull converter is presented in this paper. These features are accomplished through a partial regeneration of the energy stored in the transformer's leakage inductance with an active clamping voltage circuit performed by a buck converter. Normally, current-fed push-pull converters have an energy loss in passive snubber circuits. The converter description, operation principles, waveforms, modeling, design and the experimental results of a 2000 Watts prototype are presented. The proposed converter can be implemented in high power applications that require bidirectional power flow and galvanic isolation, such as DC microgrids and electric vehicle battery chargers.**

Index Terms – Battery charger, bidirectional DC-DC converter, buck converter, current-fed push-pull, full-bridge ZVS-PWM, isolated bidirectional.

I. Introduction

Due to the climate changes that have been occurring in recent decades, several organizations have started to look for technologies that employ renewable energy sources because of their lower environmental impact compared to fossil fuels. Most of these sources are seasonal by its nature, which require an energy storage system to supply the load in periods when there is no power being generated [1].

To charge and discharge a battery energy storage system (BESS), a bidirectional DC-DC converter is more appropriate since it has less components than two individual unidirectional DC-DC converters for each power flow direction. In addition, the galvanic isolation provided by a medium frequency transformer increases safety.

There are many topologies of isolated bidirectional DC-DC converters. However, most of them present some disadvantages as poor efficiency, high ripple current at the low voltage side and high breakdown voltage of the switches that must be suppressed using snubber circuits. Nowadays, the main topology for high power applications is the dual active bridge (DAB) converter as presented in [2], but there are other alternatives that employ the full-bridge [3], half-bridge [4], push-pull [5], and resonant converters [6]-[7].

While DAB has been deeply studied, other topologies are still a challenge. For instance, the assimilation of the full-bridge and current-fed push-pull converters cause an energy stored in the transformer's leakage inductance (L_{lk}) that adds to the reverse recovery current of push-pull switches' anti-parallel diodes. This energy is discharged on the switches' intrinsic capacitors, demanding voltage regulator circuits that decrease the converter's efficiency [8]-[9].

In this paper, we present an efficient isolated bidirectional DC-DC converter for high power applications with high static gain, low breakdown voltage across the switches and low current ripple at the low voltage side.

II. Converter Analysis

A. Power Stage Description

The converter designed by the authors in [10] is based on an integration of a DC-DC full-bridge ZVS-PWM [11] in the primary side of the medium frequency transformer and a current-fed push-pull in the secondary side, as shown in Fig. 1. This integration requires voltage clamping circuits on switches S_5 and S_6 to limit their breakdown voltages.

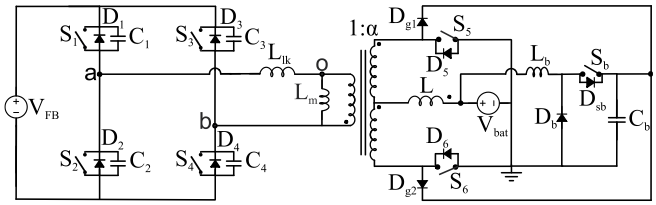


Fig. 1. Isolated bidirectional DC-DC converter proposed.

The transformer with turns ratio equals to α has a small leakage inductance, so it does not accumulate much energy, which reduce the losses in the clamping circuit. However, this inductance provides energy to charge and discharge the commutation capacitors that is necessary to achieve soft switching, which increases the converter's performance.

There are many clamping circuits to recycle the energy from the transformer leakage inductance [12]. This paper proposes a buck converter to transfer the energy accumulated in the leakage inductance back to the low voltage side instead of losing this energy to passive circuits, increasing efficiency and imposing a desirable low voltage across the switches.

B. Operation Principles

The gate signals of each switch are presented in Fig. 2, which the signals of each leg are complementary. Additionally, the voltage across the transformer's primary side (V_{ab}) and power transferred to the battery are controlled by the shift angle between the converter's legs (ϕ), which 0º represents the maximum power transfer and 180º represents zero power transfer.

The modulation is performed in order to switch S_5 gates off at the time voltage V_{ab} is negative and switch S_6 turns off when voltage V_{ab} is positive. Then, there will be no short-circuit and voltage induced in the secondary side at the same time.

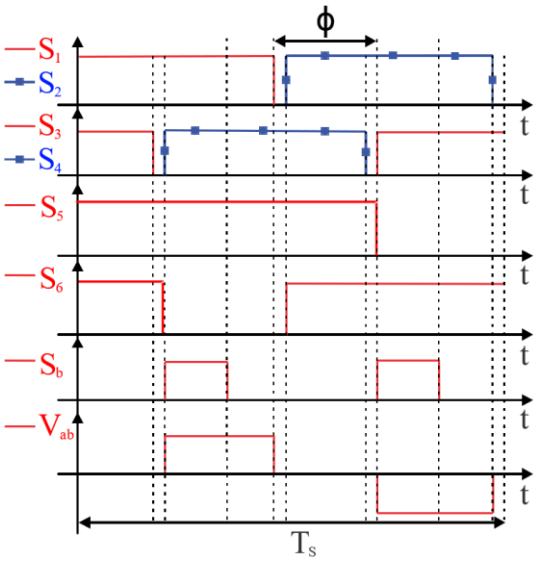


Fig. 2. Gate signals of the converter's switches.

Although buck's gate signal is synchronized with the bidirectional converter and has two times its frequency as presented in Fig. 2, the converter operates regardless this synchronism.

The bidirectional converter has two power flow directions that will be named positive and negative. The positive direction refers to power transferred from high voltage source (V_{FB}) to low voltage source (V_{bat}) and negative indicates the opposite power flow. Since topological states are symmetric for half commutation period, only seven time intervals will be necessary to understand the converter's operation for each power flow direction.

The topological states of the positive power flow are given in Fig. 3, and each time interval is described as follows:

a) **Time interval [$t_0 - t_1$]:** At time t_0, the switches S_1, S_3, S_5 and S_6 are turned on, so voltage V_{ab} is zero. However, the current in the leakage inductor (I_{Llk}) tends to flow through diode D_1 because it has a lower resistance than the MOSFET S_1. In addition, current in the secondary side (I_L) flows through switch S_6 and current stored in the inductor L_b is discharged in V_{bat}.

b) **Time interval [$t_1 - t_2$]:** This time interval represents the period which soft switching occurs. Therefore, when S_3 is gated off and S_4 has not been switched on yet, primary side current charges capacitor C_3 and discharges C_4. In addition, the secondary side is short-circuited and voltage V_{ob} is zero.

c) **Time interval [$t_2 - t_3$]:** At the instant t_2, switch S_4 is gated on. The current I_{Llk} has a negative value that gradually increases, then it flows through diodes D_1 and D_4 until reaches zero. Additionally, the anti-parallel diode D_6 of switch S_6 has a reverse recovery current that flows through diode D_{g2} because it is forward biased, charging buck's capacitor (C_b) and inductor (L_b).

d) **Time interval [$t_3 - t_4$]:** This interval begins when the current in L_{lk} is zero and starts to rise linearly. In this step, voltage V_{ob} is still zero, which represents a loss of duty cycle. In addition, current flows through switches S_1 and S_4 because current I_{Llk} has changed its direction.

e) **Time interval [$t_4 - t_5$]:** At time t_4, current I_{Llk} reaches its nominal value. Since voltage V_{ob} is not zero anymore, the power is transferred from V_{FB} to V_{bat} through switch S_5. As the energy from the reverse recovery ends and switch S_b is still turned on, the energy stored in the capacitor C_b discharges into the secondary voltage source through the inductor L_b.

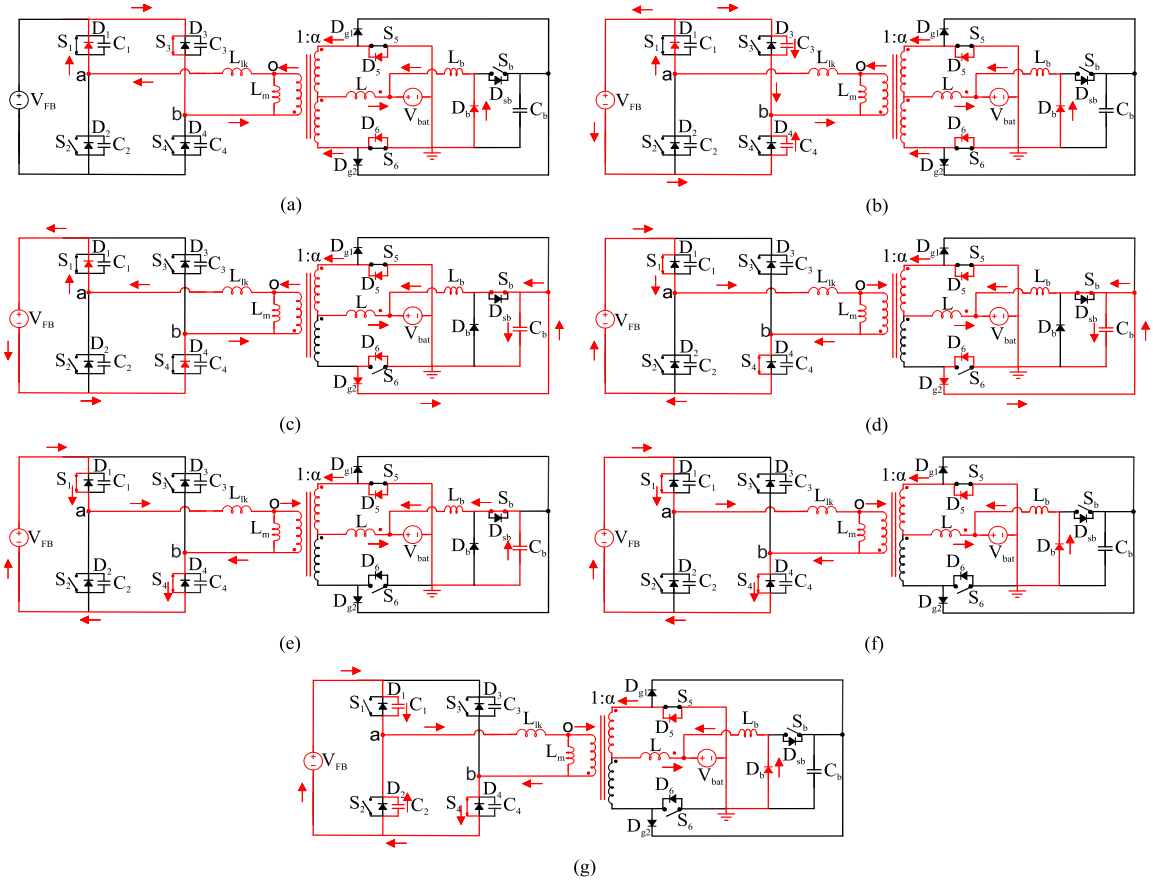


Fig. 3. Topological states of the time intervals: (a) time interval [$t_0 - t_1$], (b) time interval [$t_1 - t_2$], (c) time interval [$t_2 - t_3$], (d) time interval [$t_3 - t_4$], (e) time interval [$t_4 - t_5$], (f) time interval [$t_5 - t_6$] and (g) time interval [$t_6 - t_7$] for the positive power flow direction.

f) **Time interval [$t_5 – t_6$]:** At time t_5, switch S_b is gated off. Therefore, only the inductor L_b provides energy to the battery.

g) **Time interval [$t_6 – t_7$]:** At time t_6, there is a dead-time between switches S_1 and S_2. Then, when S_1 turns off and S_2 has not been turned on yet, the current stored in L_{lk} charges C_1 and discharges C_2. Moreover, since switch S_b is turned off, L_b provides energy to the V_{bat}.

The main waveforms of the converter operating with positive power flow direction are represented in Fig. 4, which time intervals t_0 to t_7 describe the topological states presented in Fig. 3.

In addition, the topological states of the negative power flow are given in Fig. 5, and each time interval is described as follows:

a) **Time interval [$t_0 – t_1$]:** At time t_0, switches S_5 and S_6 are gated on. Thus, there is zero voltage across V_{ab}. Since the switches S_1 and S_3 are turned on, the current I_{Llk} flows through them and at the secondary side current I_L starts to change its trajectory from switch S_6 to S_5 in a linear way because they are short-circuited.

b) **Time interval [$t_1 – t_2$]:** On this time interval switch S_3 is gated off while S_4 has not been gated on yet. Nonetheless, there is an intrinsic diode D_3 in anti-parallel with S_3 that conducts the current. Therefore, since current does not flow through the capacitors C_3 and C_4 like in the positive operation, soft commutation is not achieved.

c) **Time interval [$t_2 – t_3$]:** At the instant t_2, switch S_4 is turned on and S_6 is turned off. Thus, there is a positive voltage across V_{ab} and current I_{Llk} flows through S_1 and S_4. Additionally, when D_6 is gated off the leakage inductance energy is transferred to C_b and V_{bat} since the diode D_{g2} is forward biased.

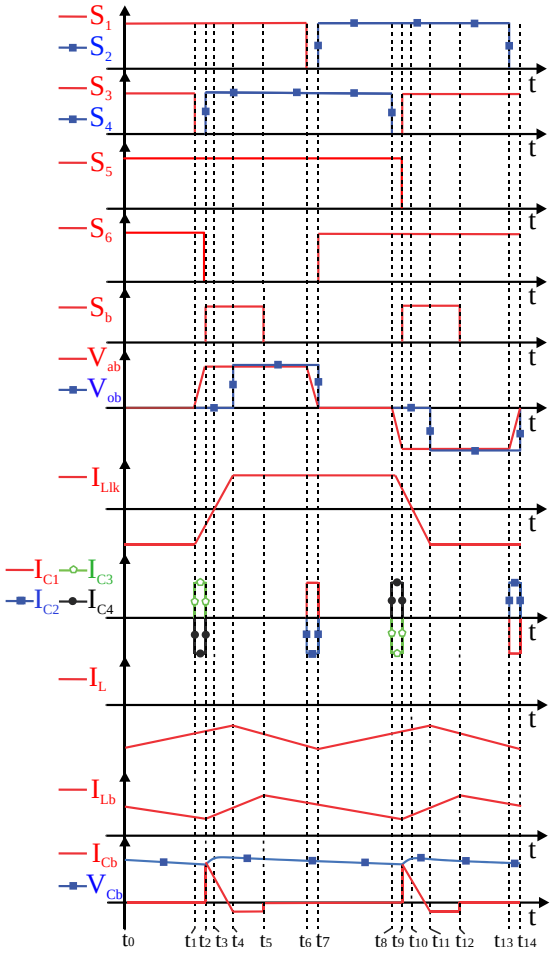


Fig. 4. Main waveforms of converter operating with positive power flow direction with time intervals t_0 to t_7 described.

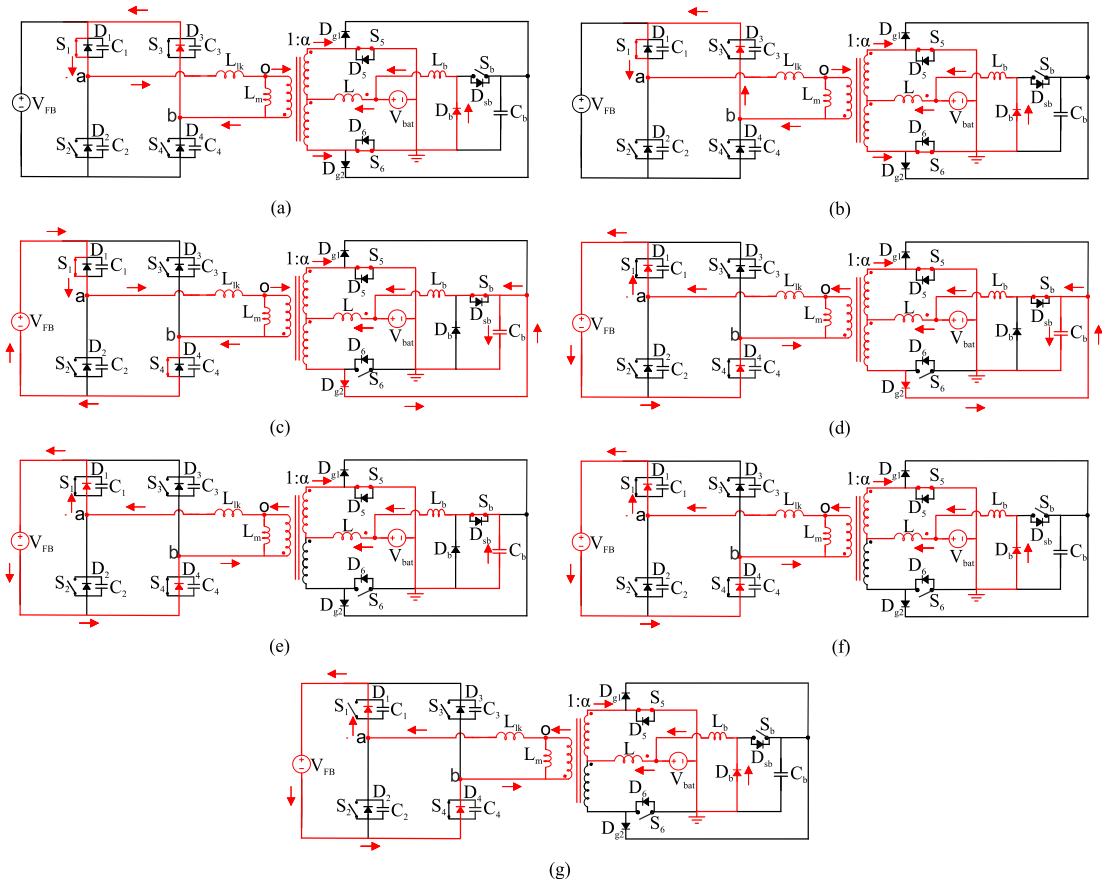


Fig. 5. Topological states of the time intervals: (a) time interval [$t_0 – t_1$], (b) time interval [$t_1 – t_2$], (c) time interval [$t_2 – t_3$], (d) time interval [$t_3 – t_4$], (e) time interval [$t_4 – t_5$], (f) time interval [$t_5 – t_6$] and (g) time interval [$t_6 – t_7$] for the negative power flow direction.

d) **Time interval [t_3 – t_4]:** On this time interval, the voltage clamping circuit is still transferring energy to V_{bat} and switch S_5 is responsible to transfer power from V_{FB} to V_{bat}. Since I_{Llk} changes its direction, the diodes D_1 and D_4 conduct the current.

e) **Time interval [t_4 – t_5]:** At time t_4, the current I_{Llk} has been completely discharged, the C_b discharges into V_{bat} to keep a steady clamping voltage on switches S_5 and S_6.

f) **Time interval [t_5 – t_6]:** At time t_5, the switch S_b is gated off. Therefore, the capacitor C_b does not provide energy to V_{bat} anymore, only L_b.

g) **Time interval [t_6 – t_7]:** At time t_6, switch S_1 turns off while S_2 has not been turned on yet. Since there are intrinsic anti-parallel diodes, I_{Llk} continues to flow through D_1 and D_4. However, in this interval, V_{ob} is zero.

In summary, Fig. 6 presents the main waveforms for the negative power flow. The voltage stresses are equal to the voltage V_{FB} on the switches S_1, S_2, S_3 and S_4, and to V_{Cb} on the switches S_5, S_6 and S_b. In addition, the current stresses are calculated with the leakage inductance current (I_{Llk}) waveform for the switches S_1, S_2, S_3 and S_4 and with the inductor current (I_L) for S_5 and S_6.

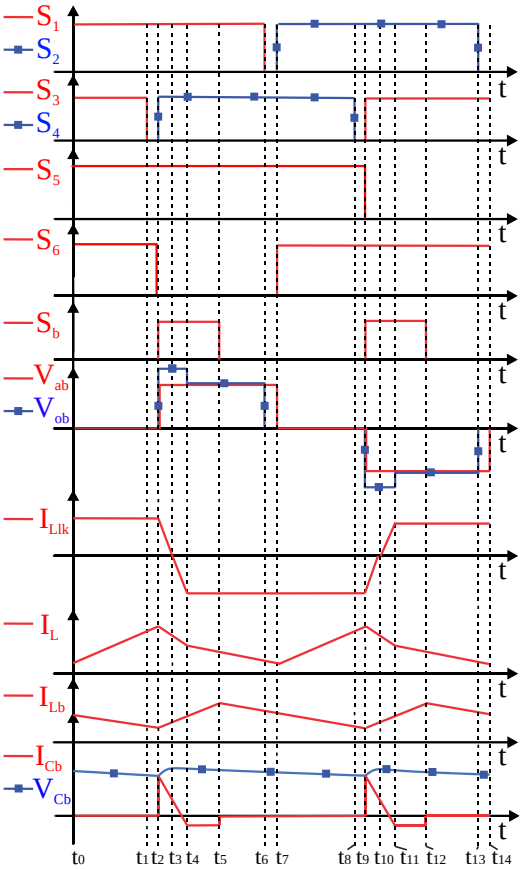


Fig. 6. Main waveforms of converter operating with negative power flow direction with time intervals t_0 to t_7 described.

C. Characteristics

The converter's duty cycle (D) is defined as the period when the inductor (L) discharges. Therefore, the main characteristics that can be derived from the converter's operation are time intervals, which are determined by

$$\Delta t_1 = (1-D)\frac{T_S}{2} \tag{1}$$

$$\Delta t_2 = \Delta t_7 = \Delta t_d \tag{2}$$

$$\Delta t_3 = \Delta t_4 = (D - D_{ef})\frac{T_S}{2} - \Delta t_d \tag{3}$$

$$\Delta t_5 = \frac{L_b I_{Lb}}{2V_{Cb}} \tag{4}$$

$$\Delta t_6 = D_{ef}\frac{T_S}{2} - \Delta t_5 \tag{5}$$

Which D_{ef} is the effective converter's duty cycle, T_S is the total switching time, Δt_d is the dead-time interval, L_b is the buck inductance, I_{Lb} is the buck inductance current and V_{Cb} is the clamping voltage.

III. Modeling and Control

Some applications require a closed-loop control system, in order to the measured variable follow a reference. Thus, the converter transfer function that relates the variation of the inductor current (I_L) with the complement duty cycle (d) is determined to project the controller. The transfer function in the frequency domain can be found through small-signal AC model, as presented in [13].

Therefore, the block diagram presented in Fig. 7 describes the inductor current closed-loop control.

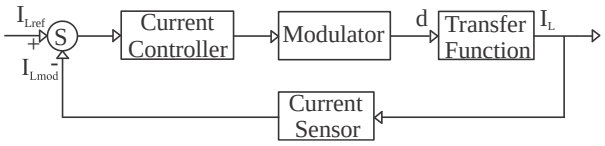


Fig. 7. Block diagram of the closed-loop current control.

To find the inductor current transfer function in relation to the complement duty cycle, the simplified equivalent circuit of the secondary side of the transformer will be analyzed. In summary, it presents two topological states shown in Fig. 8.

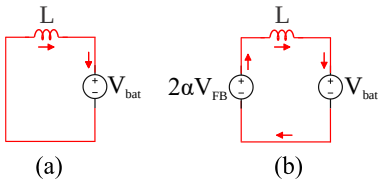


Fig. 8. Simplified equivalent circuit: (a) First topological state and (b) Second topological state.

(a) **Time interval Δt_1^* :** The first state represents the periods which the voltage across the transformer (V_{ab}) is null because both switches S_5 and S_6 are gated on, as represented on Fig. 8 (a).

(b) **Time interval Δt_2^*:** At the second topological state, the voltage in the secondary side of the transformer is not null because one of the switches is turned off, as presented on Fig. 8 (b).

Then, the voltage across the inductor for time intervals Δt_1^* and Δt_2^* are given by

$$V_L = -V_{bat} \tag{6}$$

$$V_L = 2\alpha V_{FB} - V_{bat} \tag{7}$$

Using both inductance voltage equations, it is possible to calculate the transformer's voltage as

$$V_{ab} = 2\alpha V_{FB}\left(1 - \frac{2\Delta t_1^*}{T_S}\right) \tag{8}$$

Time interval Δt_1^* can be divided into time that current stored in the leakage inductance is transferred to the voltage clamping circuit (Δt_{Llk}) and the remaining period which the voltage across the transformer is null (Δt_a).

$$\Delta t_1^* = \Delta t_a + \Delta t_{Llk} \tag{9}$$

Then, by replacing (9) into (8), the voltage V_{ab} is found to be the sum of the voltage without influence of the leakage inductance (V_{ox}) with its voltage drop.

$$V_{ab} = 2\alpha V_{FB}\left(1 - \frac{2\Delta t_a}{T_S}\right) - 2\alpha V_{FB}\left(\frac{2\Delta t_{Llk}}{T_S}\right) \tag{10}$$

$$V_{ox} = 2\alpha V_{FB}\left(1 - \frac{2\Delta t_a}{T_S}\right) \tag{11}$$

Therefore, an equivalent circuit that represents the voltage drop in the secondary side due to the leakage inductance can be found, as shown on Fig. 9.

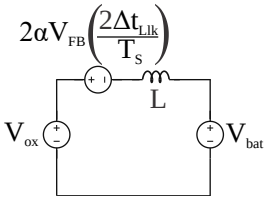


Fig. 9. Equivalent circuit with the leakage inductance voltage drop.

It is possible to replace the voltage drop of Fig. 9 with a resistance.

$$2\alpha V_{FB}\left(\frac{2\Delta t_{Llk}}{T_S}\right) = R_{Llk} I_L \tag{12}$$

To find the resistance R_{Llk}, it is required the time interval Δt_{Llk}, which is possible with the voltage across the leakage inductance (L_{lk}).

$$\Delta t_{Llk} = \frac{\alpha L_{lk} I_L}{V_{FB}} \tag{13}$$

Finally, replacing (13) in (12) leads to

$$R_{Llk} = 4\alpha^2 L_{lk} f \tag{14}$$

In addition, the complement duty cycle can be written as

$$d = 1 - D = 1 - \frac{2\Delta t_a}{T_S} \tag{15}$$

Therefore, replacing (14) and (15) in (11) gives

$$V_{ab} = 2\alpha V_{FB} d - 4\alpha^2 L_{lk} I_L f \tag{16}$$

Additionally, it is possible to substitute (16) in (11) to find a new equivalent circuit, as shown in Fig. 10.

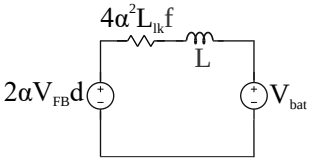


Fig. 10. Equivalent circuit with the resistance of the leakage inductance.

Then, by applying the Kirchhoff Voltage Law in the new equivalent circuit the following equation is found.

$$2\alpha V_{FB} d = V_{bat} + 4\alpha^2 L_{lk} I_L f + L\frac{dI_L}{dt} \tag{17}$$

It is desirable to obtain the transfer function of the current (I_L) in relation to the complement duty cycle (d). So, a perturbation is applied in those variables as follows

$$d = d + \overline{\Delta d} \tag{18}$$

$$I_L = I_L + \overline{\Delta I_L} \tag{19}$$

Now, replacing (18) and (19) in (17) leads to

$$2\alpha V_{FB}(d + \overline{\Delta d}) = V_{bat} + 2L_{lk} f\left(I_L + \overline{\Delta I_L}\right) + L\frac{d\left(I_L + \overline{\Delta I_L}\right)}{dt} \tag{20}$$

Therefore, by applying the Laplace Transform and doing some algebraic manipulations, the transfer is found.

$$\frac{I_L(s)}{d(s)} = \frac{2\alpha V_{FB}}{sL + 4\alpha^2 L_{lk} f} \tag{21}$$

Finally, a bode diagram is plotted with the model and simulated curves, as shown in Fig. 11. The value of each variable will be presented in section IV.

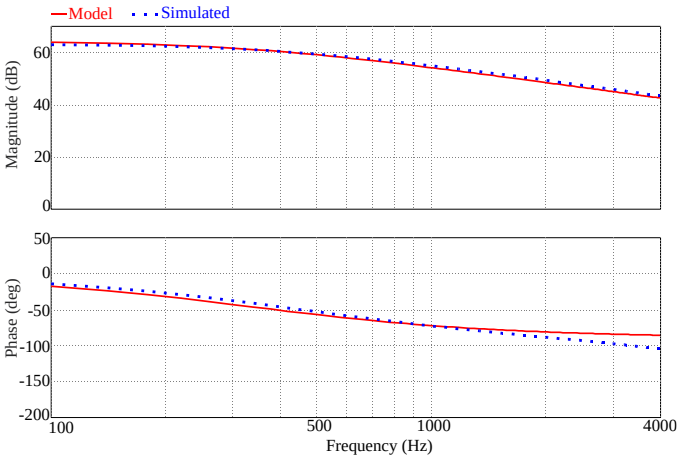


Fig. 11. Bode diagram of the model and simulated inductor current transfer function.

IV. Experimental Resultas and Analysis

In order to validate the theoretical analysis, an experimental prototype was developed, as shown in Fig. 12, following the specifications shown in Table I.

A. Design

Basically, the transformer's leakage inductance causes a lost in the duty cycle (ΔD) that is stipulated. Then, for a duty cycle (D) equals to 0.7, the effective duty cycle (D_{ef}) is calculated as

$$D_{ef} = D - \Delta D = 0.65 \tag{22}$$

TABLE I. SPECIFICATIONS OF THE PROPOSED CONVERTER

Specification	Symbol	Value
Rated Power	P_{out}	2000 W
Primary Side Voltage	V_{FB}	400 V
Secondary Side Voltage	V_{bat}	48 V
Clamping Voltage	V_{Cb}	220 V
Switching Frequency	f	40 kHz
Clamping Circuit Frequency	f_b	80 kHz
Minimum Power to Achieve ZVS	P_{min}	800 W
Duty Cycle Loss	ΔD	0.05
Series Capacitor Voltage Drop	ΔV_{Cr}	2.5 %
Clamping Capacitor Ripple Voltage	ΔV_{Cb}	1 %
Inductor Ripple Current	ΔI_L	10 %
Clamping Inductor Ripple Current	ΔI_{Lb}	10 %

The next equations are deducted in [10]. The transformer turns ratio can be calculated as

$$\alpha = \frac{V_{bat}}{V_{FB} D_{ef}} = 0.185 . \tag{23}$$

The current in the leakage inductance is given by

$$I_{Llk} = \frac{\alpha P_{out}}{V_{bat}} = 7.692A \tag{24}$$

Furthermore, the leakage inductance is calculated as

$$L_{lk} = \frac{V_{FB} \Delta D}{4 I_{Llk} f} = 16.25\mu H \tag{25}$$

In addition, a capacitor in series with the leakage inductance is necessary to filter the DC level resulted from the commutation inequality of all the switches. This capacitor does not change the topological states and is determined by

$$C_r = \frac{I_{Llk}}{2\alpha f \Delta V_{Cr} V_{FB}} = 9.65\mu F \tag{26}$$

To achieve soft commutation, capacitors have to be placed in parallel with the MOSFETs in the primary side and a dead-time applied. The minimum capacitance is represented by

$$C_{\min} = \left(\frac{P_{\min}}{V_{FB}^2 D_{ef}} \right)^2 . \frac{L_{lk}}{2} = 0.48nF \tag{27}$$

However, the commutation capacitance must consider the MOSFET intrinsic capacitance according to the component's datasheet. Therefore, with the sum of both capacitances, the commutation capacitance (C_c) is used to calculate the dead-time.

$$\Delta t_d = \left[\frac{\pi}{2} - \cos^{-1}\left(\frac{V_{FB}^2 D_{ef}}{P_{\min}} . \sqrt{\frac{2C_c}{L_{lk}}} \right) \right] . \left(\sqrt{2 L_{lk} C_c} \right) = 221ns \tag{28}$$

The current in the inductor at the secondary side is given by

$$I_L = \frac{P_{out}}{V_{bat}} = 41.667A \tag{29}$$

The inductance value can be calculated using the current ripple criteria

$$L = \frac{V_{bat}(1-D)}{2 f I_L \Delta I_L} = 43.2\mu H \tag{30}$$

The buck converter that will be used as a clamping circuit to limit the voltage across MOSFETs S_5 and S_6 can be sized according to the power that should be recovered. The buck's duty cycle presented in (31) varies according to the desirable clamping voltage, which the limit must be the MOSFETs breakdown voltage.

$$d_b = \frac{V_{bat}}{V_{Cb}} = 0.218 \tag{31}$$

Additionally, the time that the clamping diodes are forward biased (Δt_g) can be calculated as

$$\Delta t_g = \frac{I_{Llk} L_{lk}}{2 V_{FB}} = 156ns \tag{32}$$

With the time necessary to the current reaches its maximum value, it is possible to calculate the maximum current through the clamping diode (I_{Dg}) as

$$I_{Dg} = \frac{V_{Cb} \Delta t_g}{2 L_{lk} \alpha^2} = 31A \tag{33}$$

The current that charges the capacitor is provided by two clamping diodes and has a triangular waveform. Therefore, the power that the clamping circuit process is obtained as

$$P_{buck} = 2 f_b \int_0^{\Delta t_g} I_{Dg} V_{Cb} dt = 170W \tag{34}$$

The Buck converter was designed to transfer up to 200 W. Thus, the average current on its inductor can be calculated as

$$I_{Lb} = \frac{P_{buck}}{V_{bat}} = 4.167A \tag{35}$$

The buck inductor can be calculated using the ripple current.

$$L_b = \frac{V_{bat}\left(V_{Cb} - V_{bat}\right)}{f_b V_{Cb} I_{Lb} \Delta I_{Lb}} = 0.45mH \qquad (36)$$

In order to size buck's capacitor, it is necessary to calculate its RMS current (I_{Cbrms}), which is represented as

$$I_{Cbrms} = 2\sqrt{f\int_0^{\Delta t_3 + \Delta t_4}\left(\frac{I_{Dg}}{2}\right)^2 dt} = 5.517A \qquad (37)$$

Therefore, capacitor C_b can be sized with the voltage ripple criteria as presented in (38). The RMS current must be smaller than the maximum presented in the component's datasheet.

$$C_b = \frac{I_{Cbrms} d_b}{f V_{Cb} \Delta V_{Cb}} = 13.667\mu F \qquad (38)$$

The final prototype is shown in Fig. 12. All the necessary circuits and components are presented in [10]. In addition, the inductors and transformer were built by the author.

Fig. 12. Power stage of the experimental prototype of the proposed bidirectional isolated dc-dc converter.

B. Experimental Results

The experimental results were obtained by debugging the prototype for each power flow direction. Therefore, Fig. 13 represents the voltage on both sides.

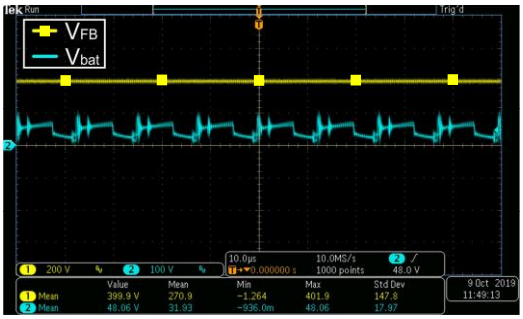


Fig. 13. Primary side (V_{FB}) and secondary side (V_{bat}) voltages.

In addition, Fig. 14 shows the Zero Voltage Switching for the positive power flow direction, since S_4 has no voltage across its terminals when the gate signal is generated.

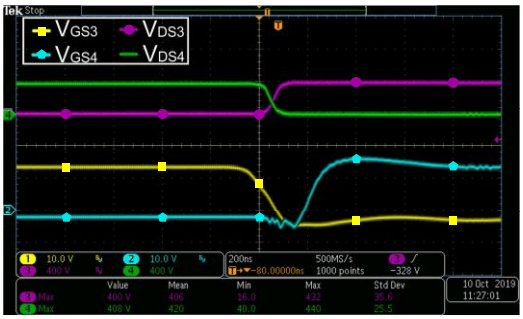


Fig. 14. Gate signals and breakdown voltage across switches S_3 and S_4 to prove soft switching in the positive power flow.

The clamping voltage shown in Fig. 15 can be set by changing the buck's duty cycle. Furthermore, V_{DS5} and V_{DS6} are the voltages across the switches S_5 and S_6, respectively.

Fig 15. Clamped voltage across switches S_5 and S_6 (V_{DS5} and V_{DS6}) with its clamping capacitor voltage (V_{Cb}).

The current and voltage across transformer's primary side for both power flows are presented on Fig. 16 and Fig. 17, respectively. Note that differences between experimental and theoretical currents are due to gate signal delays between the switches, in practical experience, that inserted unpredicted topological states in the converter operation.

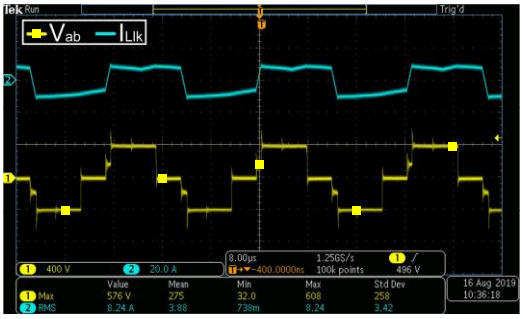


Fig. 16. Voltage across the transformer (V_{ab}) and leakage inductor current (I_{Llk}) for the positive power flow direction.

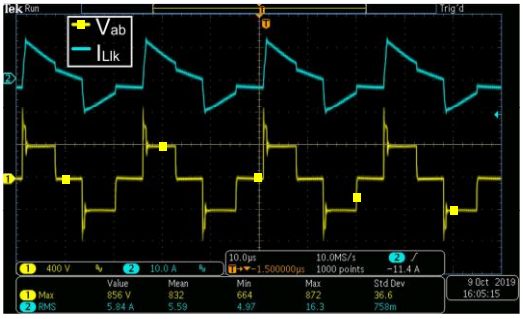


Fig. 17. Voltage across the transformer (V_{ab}) and leakage inductor current (I_{Llk}) for the negative power flow direction.

The main current waveforms for the positive and negative power flows are presented in Fig. 18 and Fig.19, respectively.

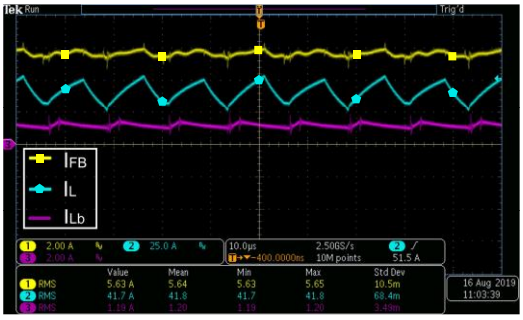


Fig. 18. Primary side (I_{FB}), secondary side (I_L) and clamping inductor (I_{Lb}) currents for the positive power flow direction.

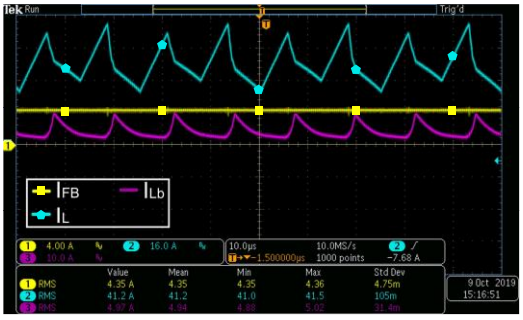


Fig. 19. I Primary side (I_{FB}), secondary side (I_L) and clamping inductor (I_{Lb}) currents for the negative power flow direction.

Finally, the converter's efficiency was acquired for both power flows. In fact, for the positive power flow, two different set ups that considered hard and soft commutation were applied. Finally, Fig. 20 describes the converter's efficiencies as a function of the processed power.

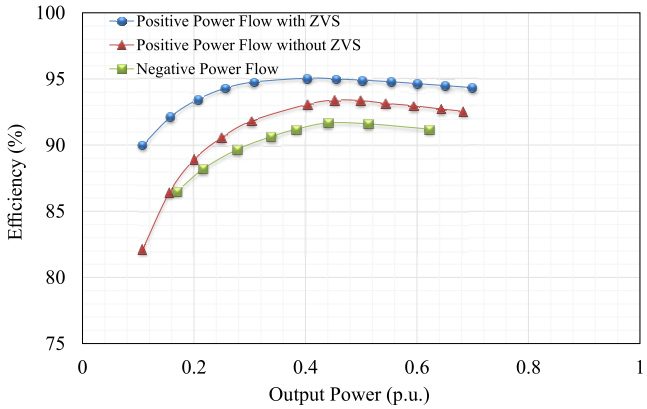


Fig. 20. Converter's efficiency for positive and negative power flows.

The maximum efficiency of 95.1% was acquired for the positive and 91.8% for the negative power flow. The experiments without soft commutation decrease the converter's performance by 2%, which explain one reason that contributes to reduce the efficiency for the negative power flow.

V. Conclusion

This paper presents an alternative for bidirectional isolated DC-DC converter with high static gain based on the integration of the full-bridge ZVS-PWM and current-fed push-pull converters. The topology requires a clamping circuit to reduce the voltage across the power semiconductors of the secondary side and regenerate energy stored in the transformer leakage inductance. Therefore, by using a low power buck converter as an active voltage clamping, the bidirectional converter can be designed to operate with high efficiency and low breakdown voltage. The higher efficiencies acquired were 95.1% and 91.8% for the positive and negative power flow, for a non-optimized experimental prototype, which is an advantage among similar converters. Moreover, the experimental results obtained with a 2000 Watts prototype evidenced the converter's performance with low ripple current at the low voltage side, authenticating this topology for isolated bidirectional DC-DC applications.

Acknowledgment

The authors would like to thank the Strategic Research Group on Solar Energy at UFSC and the Brazilian Institute of Power Electronics and Renewable Energies for providing the necessary components and equipment on the elaboration of the prototype. In addition, acknowledgement is made for the staff support from both research groups.

References

[1] M. Upasani and S. Patil, "Grid connected solar photovoltaic system with battery storage for energy management", in 2018 2nd International Conference on Inventive Systems and Control (ICISC), pp. 438-443, Jan. 2018.

[2] H. Daneshpajooh, A. Bakhshai, and P. Jain, "Modified dual active bridge bidirectional DC-DC converter with optimal efficiency," in Proc. IEEE 27th Annu. Appl. Power Electron. Conf. Expo., 2012, pp. 1348– 1354.

[3] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS–PWM DC–DC converter for bidirectional high power applications," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 422–429, Mar. 2006.

[4] F. Z. Peng, H. Li, G. J. Su, and J. S. Lawler, "A new ZVS bidirectional dc-dc converter for fuel cell and battery application," IEEE Trans. Power Electron., vol. 19, no. 1, pp. 54–65, Jan. 2004.

[5] M. Jain, M. Daniele, and P. K. Jain, "A bidirectional dc-dc converter topology for low power application," IEEE Trans. Power Electron., vol. 15, no. 4, pp. 595–606, Jul. 2000.

[6] Gu, L., & Li, P., "Hybrid PWM Control of Bidirectional DC/DC Resonant Converter for Low-Current-Ripple and Wide-Voltage-Gain Application," IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2158-2162, Mar. 2020.

[7] Zeng, Yangbin, et al. "A Parallel-Resonant Isolated Bidirectional DC-DC Converter with Low Current Ripple for Battery Storage Systems." IEEE Energy Conversion Congress and Exposition (ECCE), 2019.

[8] K. Dadialla and R. S. Hardas, "Development of prototype model of DC-DC bi-directional converter." IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), pp. 1620-1623, June 2017.

[9] G. Chen, Y. Deng, H. Peng, X. He and Y. Wang, "An optimized modulation method tor full-bridge/push-pull bi-directional DC-DC converter with wide-range ZVS and reduced spike voltage," IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, 2014, pp. 1247-1253.

[10] Y. P. Marca, *"Isolated Bidirectional DC-DC Converter Based on the Integration of the Full-Bridge ZVS-PWM and Current-Fed Push-Pull Converters for DC Microgrid"*, Federal University of Santa Catarina, Master Thesis, Florianopolis, 2019.

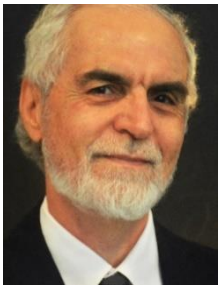
[11] I. Barbi and F. Pottker, *Soft Commutation Isolated DC-DC Converters*, Springer International Publishing, 1 ed., 2019.

[12] F. J. Nome and I. Barbi, "A ZVS clamping mode-current-fed push-pull DC-DC converter", IEEE International Symposium on Industrial Electronics. Proceedings, Vol. 2, pp. 617-621, 1998.

[13] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Springer Science Business Media, 2nd ed., 2001.

YGOR PEREIRA MARCA was born in Ji-Paraná, Brazil. He received the B.Sc. degree in electrical engineering from the Federal Technological University of Parana (UTFPR), Curitiba, Brazil, in 2017 and the M.Sc. degree in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 2019.

He is currently working toward the Ph.D. degree at the Department of Electrical Engineering in the Group Electromechanics and Power Electronics at Eindhoven University of Technology (TU/e). His research interests include DC microgrids, electric vehicle chargers, high-power converters, isolated bidirectional DC-DC converters, soft switching and applications of renewable energy sources to decrease the environmental impact of energy production.



IVO BARBI (Life Fellow, IEEE) was born in Gaspar, Brazil. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree in electrical engineering from the Institut National Polytechnique de Toulouse (INPT), Toulouse, France, in 1979. He founded the Brazilian Power Electronics Society (SOBRAEP), the Brazilian Power Electronics Conference (COBEP), in 1990, and the Brazilian Power Electronics and Renewable Energy Institute (IBEPE), in 2016. He is currently a Researcher with the Solar Energy Research Center and a Professor Emeritus in electrical engineering with UFSC. Prof. Barbi received the 2020 IEEE William E. Newell Power Electronics Award. He was an Associate Editor for the IEEE Transactions on Industrial Electronics and the IEEE Transactions on Power Electronics, for several years.