# A Single-Event Transient (SET) Tolerant Dynamic Bias Comparator in 65-nm CMOS

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***Abstract*—A single-event transient (SET) tolerant dynamic bias comparator leveraging path-splitting is presented in this paper. The dynamic bias structure with a tail capacitor is found to be vulnerable to positive and negative SET transients. A negative transient on the tail transistor doubles the energy per conversion. A positive transient on the tail MOS capacitor reduces the preamplifier gain by 35.7%, which increases the metastability error rate in the subsequent latch. A path splitting technique is applied to mitigate the positive SET. Simulations in a 65-nm CMOS process showed that a two path split can recover the comparator output voltage swing by 12.7%. Compared with the state-of-the-art CMOS radiation-hardened by design (RHBD) dynamic comparators, this circuit achieved the lowest energy per comparison while maintaining low input referred noise and gaining SET tolerance in the evaluation phase.**

***Index Terms*—single-event transient (SET), radiation-hardened by design (RHBD), dynamic biasing, dynamic comparator, path splitting**

## I. Introduction

Robust electronics for intense radiation environments are an important consideration for reliable device performance in space, nuclear reactors, and other high radiation environments. Considering this, improving the radiation hardness of modern, high-performance circuits is a critical area of research. ADCs are a key part of instrumentation for devices exposed to harsh radiation environments, with successive approximation register (SAR) ADCs being of particular interest due to their energy efficiency and ability to take advantage of process scaling for better performance at the cost of moderate resolution and speed. A core component of SAR ADC design is the comparator which limits resolution due to thermal noise.

Comparator design is an area where radiation hardness needs an update to improve circuit efficiency. Dynamic bias comparators are a family of modern comparators capable of low energy comparisons along with good noise characteristics making them great candidates for use in SAR ADCs. This work focuses on the dynamic bias comparator proposed in [1]. This particular design was selected for radiation hardening as a SAR ADC [2] using it was able to achieve a record low Walden FoM of 0.35 fJ per conversion step as shown in Fig. 1.

The contributions of this work are as follows:

- A single-event transient (SET) vulnerability in the biasing structure of the dynamic bias comparator is identified
- A path splitting solution is applied to the dynamic bias comparator to resolve the SET vulnerability and validated via simulation

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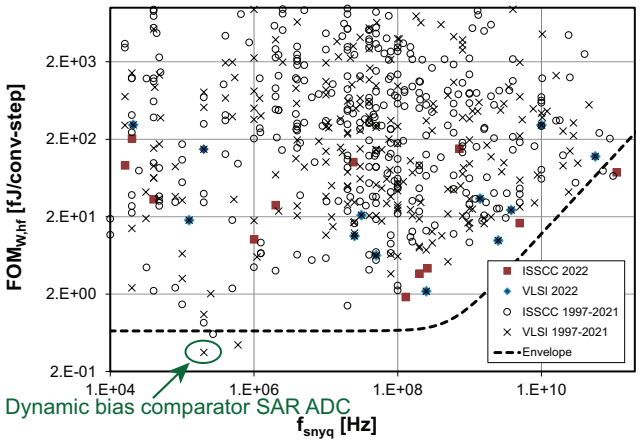


Fig. 1. Walden FoM for 25 years of ADC designs [3]. The dynamic bias comparator is used in the SAR ADC [2] with the lowest FoM.

The rest of the paper is organized as follows. Section II reviews the related works this paper builds on. Section III offers details on the design and expected performance improvement. Section IV shows the design performance in SPICE simulations. Section V summarizes the findings.

## II. Related Works

### A. Radiation Effects

There are two primary categories of concern for electronics in high radiation environments, total ionizing dose (TID) and single-event effects (SEEs). TID causes shifting of key MOSFET properties such as threshold voltage and leakage currents which lead to changes in device performance; fortunately, the parameter shift is greatly reduced for modern process sizes [4]. In addition, TID effects can be further reduced by using alternative transistor topologies such as enclosed gate layout [5]. Because of these established methods to limit TID, this work does not consider TID effects.

SEEs occur when a high energy particle travels into a semiconductor device. Electron-hole pairs are released in the device as the particle travels [6]; this charge creates a transient current pulse that can introduce many different errors to a

circuit. A single-event transient (SET) occurs when a signal path is hit, and the intended signal is distorted or entirely lost. An SET passing near or through the drain of a MOSFET into the bulk will create a temporary current between the two [7]. A strike in the vicinity of a MOS capacitor results in electrons or holes being collected which will increase or decrease the voltage across the capacitor [8] [9].

### *B. Radiation Hardening by Design*

Before looking at radiation hardening by design, it is important to acknowledge there is another option to consider. Radiation hardening by process uses alternative substrate materials that have a more robust response to radiation [10]. These alternative processes tend to be costly and can negatively impact performance in power, area, and speed. For these reasons, the alternative of radiation hardening by design was selected.

An early radiation-hardened comparator was proposed in [11]. The design used an auto-zeroing technique to limit an SET's influence to a single evaluation period. [12] and [13] describe a technique to improve the radiation response of switched-capacitor circuits. The path involving the critical capacitor(s) is split into two separate, identical paths in parallel with transistor and capacitor sizes cut in half. Under normal conditions, the split path circuit behaves identically to the original; however, during SETs, there is an alternative path for current to continue to flow. Recently [14] moved radiation-hardened comparator design forward by improving a double-tail dynamic comparator with a radiation-hardened latch. SETs on most nodes could be quickly cleared from the system by additional paths in the latch capable of forcing faulty voltages back to the proper state.

### *C. The Dynamic Bias Comparator*

The dynamic bias comparator (preamplifier shown in Fig. 2a), originally proposed in [1], is designed for low power consumption. The power savings are achieved in the preamplifier by using $C_{Tail}$ to prevent $V_{Di+}$ and $V_{Di-}$ from fully discharging to ground as they would in traditional designs. The change in common mode voltage can be expressed as (1) with $I_{CM}$ as the common mode current running through either input transistor. The preamplifier gain can then be expressed as (2) where $V_t$ is the thermal voltage and n (the weak-inversion slope factor) is assumed to be approximately 1.3. Although the energy savings from $C_{Tail}$ are valuable, $C_{Tail}$ also introduces a new SET vulnerability to the comparator.

$$\Delta V_{Di,CM}(t) = \frac{1}{C_P}\int_0^t I_{CM}(\tau)\,d\tau \tag{1}$$

$$A_v(t) = \frac{\Delta V_{di}}{\Delta V_{in}} = \frac{\Delta V_{Di,CM}(t)}{n \cdot V_t} \tag{2}$$

## III. Vulnerability and Proposed Solution

### *A. Negative SET*

If an SET hits the drain of $M_{5a}$ or $C_{Tail}$ and causes a decrease in the capacitor voltage, the result is not too problematic.

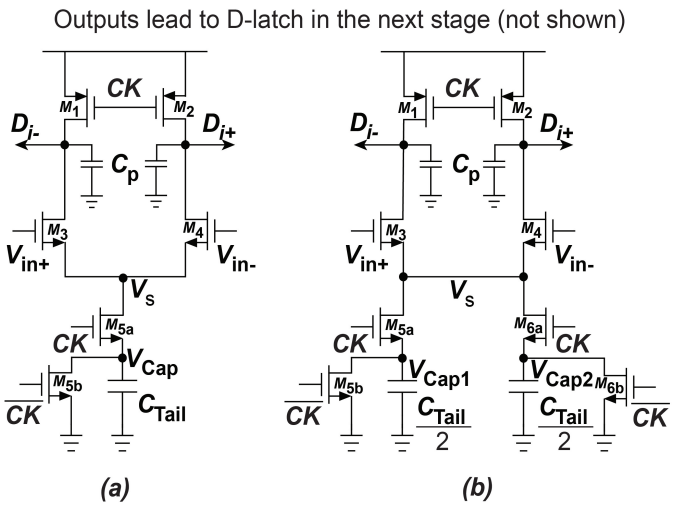


Fig. 2. a) The unhardened preamplifier for the dynamic bias comparator. b) The path splitting method applied to the preamplifier.

$V_{Tail}$ and by extension $V_s$ will be decreased. This causes $I_{CM}$ to increase and, based on (1), $\Delta V_{Di,CM}$ follows. Finally, (2) shows the preamplifier gain increases, indicating the D-latch will resolve faster. Unfortunately this comes at the cost of the comparator's low energy per comparison. Between each comparison, $D_{i+}$ and $D_{i-}$ must be recharged to the supply voltage. Extra energy will be used by the preamplifier during the next reset phase dependent on the reduction in $V_{Cap}$ due to the SET. Although these SETs do affect device performance, the transient does not force an erroneous output. In applications where the temporary increased power consumption is acceptable, no action is necessary.

### *B. Positive SET*

When an SET occurs on the MOS based tail capacitor, if the result is an increase in $V_{Cap}$, the preamplifier may propagate an error. $I_{CM}$ decreases as the difference between the common mode input voltage and $V_s$ decreases. This means that the increase in $V_{Cap}$ (and $V_s$) caused by the collected charge on $C_{Tail}$ forces $I_{CM}$ to prematurely decrease. From (1) and (2) it follows that the gain is reduced as well. The differential voltage at the inputs to the D-latch is decreased and the common mode voltage is increased, which leads to slower latch resolution and increased odds of a metastability error.

To combat the increased metastability error rate, a split path design is applied (Fig. 2b). The sizing of $M_{5a}$, $M_{5b}$, and $C_{Tail}$ are halved and made into two parallel paths ($M_5$ and $M_6$) to maintain nearly identical performance under normal conditions. Provided the two tail capacitors are kept spatially separate to mitigate charge sharing [15], a single SET is unlikely to affect both capacitors. Even if one path is blocked by a strike, there will still be a path for $D_{i-}$ and $D_{i+}$ to discharge through the other $C_{Tail}$, albeit at a slower rate. This change comes at minimal cost to power, area, and speed; the most noticeable impact is additional routing for the split path.

Additional alternative paths can be included in the design to further improve the circuit's response to an SET. By reducing $M_{5a}$, $M_{5b}$, and $C_{Tail}$ to a quarter of their original sizes, the circuit will continue to maintain performance like the original design now with four separate paths. This change adds further layout complexity, but impacts to power and area are minimal. With one struck node three other paths can continue operating, meaning circuit behavior stays closer to expected behavior. But as will be seen in section IV, the additional improvement for extra paths is less than the improvement from one path to two paths.

## IV. Simulation Results

### A. Simulation Methodology

Design validation was done using Cadence Virtuoso. To simulate an SET the double exponential current model [7] shown in (3) was used.

$$I_{SET} = \frac{Q}{\tau_f - \tau_r}(e^{-t/\tau_f} - e^{-t/\tau_r}) \tag{3}$$

Q is the deposited charge, t is time, $\tau_r$ is the ion track creation constant, and $\tau_f$ is the junction collection constant defined as (4).

$$\tau_f = \frac{\kappa \cdot \epsilon_0}{q \cdot \mu \cdot N_D} \tag{4}$$

$\kappa \cdot \epsilon_0$ is the permittivity of silicon, q is the charge of an electron, $\mu$ is electron mobility, and $N_D$ is the doping density.

[16] offers strategies to select reasonable values for simulation accuracy. They show that for 65 nm processes a $\tau_r$ value five times smaller than $\tau_f$ maintains accurate simulations. Using a technique from [17] and assuming a linear energy transfer of 15 MeV·cm$^2$/mg, a deposited charge of 71 fC is selected. According to [9] the double exponential model is not as accurate for strikes on MOS capacitors; however, for initial validation, the model will be applied to strikes on $M_{5a}$, $M_{5b}$, and $C_{Tail}$ to approximate charge distribution and collection.

### B. Simulation Results

In all simulations the following values are used: 1.2 V supply, common mode voltage of 700 mV, differential voltage of 1 mV, deposited charge of 71 fF, operating frequency of 1 GHz, and SET occurring at the beginning of the first evaluation phase (t=0). These values represent a worst case scenario (for the selected linear energy transfer), giving the SET the maximum capability to introduce errors. Simulations are run in a noise-free environment without mismatch to isolate the performance changes due to SETs.

*1) Negative SET:* The additional energy consumption of an SET that strikes the tail transistor ($M_{5a}$) is summarized in Table I and compared to a strike on the StrongARM [18] tail transistor. Performance of the StrongARM comparator is not altered much during an SET, some additional current flows and the energy is impacted accordingly. A strike on $M_{5a}$ in the dynamic bias comparator has a much larger impact, with double the normal energy per conversion. Fortunately, as noted in III.B, this strike location is inherently radiation tolerant and no errors occur. Strikes on or near $C_{Tail}$ that reduce the voltage across the capacitor have nearly identical performance to a strike on $M_{5a}$ across all three dynamic bias comparators.

*2) Positive SET:* For comparison, the response of a StrongARM comparator [18] to a negative SET on the tail transistor is simulated in a 65 nm process. Fig. 3 shows the response to the resulting increase in the common mode current. There is no meaningful difference between the evaluation during an SET and the normal performance during the next evaluation indicating inherent SET tolerance on the tail transistor.

In Fig. 4 a positive SET strikes $C_{Tail}$ for the original dynamic bias comparator design. When the SET strikes at the beginning of the evaluation period, the design's vulnerability is apparent. By the end of the evaluation $V_{Out-}$ is only able to reach 867 mV (approximately 2/3 $V_{DD}$). The reason for this can be found in the $V_{Di+,-}$ plot; the common mode voltage at the inputs to the D-latch has only dropped by 450 mV whereas during normal operation the drop is approximately 700 mV (reducing preamplifier gain by 35.7%). The higher voltage inputs to the D-latch and lower gain limit the current able to flow and reduce the resolution speed.

Fig. 5 shows a positive SET on $C_{Tail}$ for the path splitting improvement. $V_{Out-}$ in the two path design was able to achieve 977 mV (an increase of 12.7%) and the four path reached 1.03 V (an increase of 18.8%). The $V_{Di+,-}$ results show what has changed. Path splitting was able to achieve a common mode drop of 467.9 mV and 483.4 mV for two and four paths respectively; a small change in the common mode voltage leads to a noticeable improvement in the output. It is important to note the diminishing return of additional path splitting past the first change from one path to two. The first change offered 110 mV of improvement while four paths only offered an additional 53 mV of improvement.

The results of a positive SET on a MOS capacitor based $C_{Tail}$ are summarized in Table II. The outputs of a comparator are typically sent to a flip-flop or similar digital storage element. Voltage levels nearer to $V_{DD}\backslash 2$ are more likely to be incorrectly identified and stored as a bit error. The 12.7%

TABLE I
Energy Consumption During Negative SET

| Comparator | Normal (fJ/conv.) | Tail Transistor (fJ/conv.) | Energy Increase (%) | Logic Error |
|---|---|---|---|---|
| StrongARM | 99.9 | 120.5 | 20.6 | No |
| Unhardened | 62.6 | 126.2 | 101.6 | No |
| Two-Path | 61.7 | 126.8 | 105.5 | No |
| Four-Path | 64.0 | 126.8 | 98.1 | No |

TABLE II
Circuit Performance During Positive SET

| Comparator | Output Swing (V) | Improvement from Unhardened (%) |
|---|---|---|
| Unhardened | 0.867 | - |
| Two-Path | 0.977 | 12.7 |
| Four-Path | 1.03 | 18.8 |

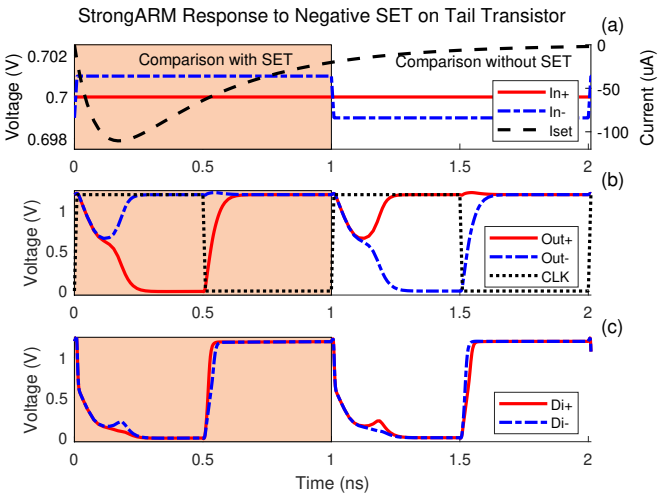


Fig. 3. Response of StrongARM comparator to negative SET on tail transistor: (a) inputs and SET current, (b) outputs and clock, (c) latch inputs.

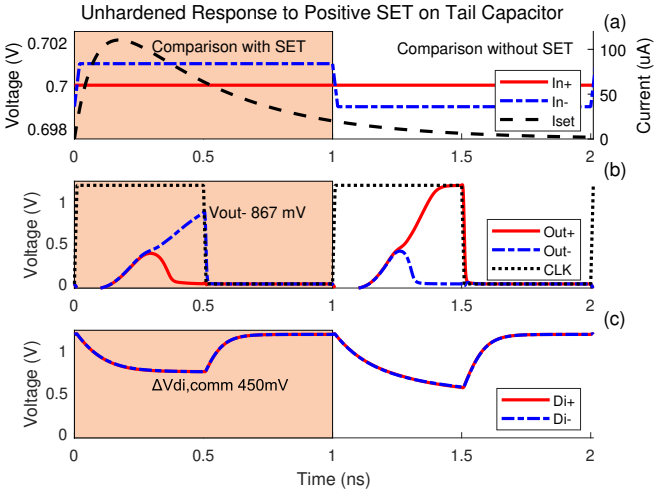


Fig. 4. Response of unhardened dynamic bias comparator to positive SET on $C_{Tail}$: (a) inputs and SET current, (b) outputs and clock, (c) latch inputs.

and 18.8% increase in voltage at the end of the evaluation period for the split path designs indicates an improvement in the deposited charge required to generate a metastability error due to an SET.

*3) Comparison to Other Works:* Table III compares the proposed two-path dynamic bias comparator design to other radiation-hardened comparators, the StrongARM [18] comparator simulated in a 65 nm process, and the original dynamic bias comparator [1]. Among SET tolerant comparators this work has the best energy per conversion. Because of the auto-zeroing technique used in [11] the input offset is low, but the SET tolerance only limits errors to a single clock cycle rather than working to entirely prevent SET errors. The performance of [14] struggles with input offset due to the many additional transistors in the modified latch increasing mismatch. The proposed design also has a large input offset; fortunately, well

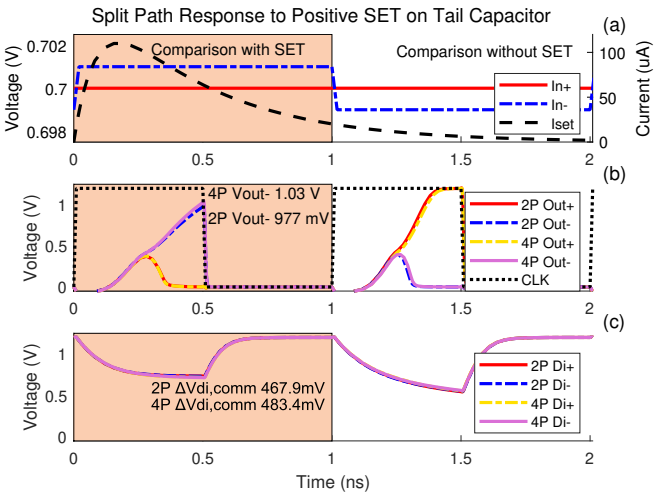


Fig. 5. Response of two and four path dynamic bias comparator to positive SET on $C_{Tail}$: (a) inputs and SET current, (b) outputs and clock, (c) latch inputs.

TABLE III
PRIOR ART COMPARISON

| Publication | This Work* | [14]* | [11]* | [18]* | [1] |
|---|---|---|---|---|---|
| Process (nm) | 65 | 55 | N/A[a] | 65 | 65 |
| Supply (V) | 1.2 | 1.2 | 2.5 | 1.2 | 1.2 |
| Clock (MHz) | 1000 | 1000 | 150 | 1000 | 25 |
| Energy per Conversion (fJ) | 61.7 | 77 | 3000 | 99.9 | 34 |
| Power (μW) | 61.7 | 77 | 450 | 99.9 | 0.85 |
| Area (μm2) | 105.2 | 57.5 | N/A[a] | 5 | 125 |
| Input Offset (mV) | 14.74 | 11.5 | 0.125 | 3.79 | N/A[a] |
| Input Referred Noise ($mV_{rms}$) | 0.5 | N/A[a] | N/A[a] | 0.14 | 0.4 |
| SET Tolerant | Yes | Yes | Yes | No | No |

*Simulation only [a]Data not disclosed

established offset cancellation techniques can be applied to reduce the impact of mismatch. Finally, the input referred noise of the radiation tolerant dynamic bias comparator is only 0.1 $mV_{rms}$ higher than that of the unhardened design. The split-path dynamic bias comparator is able to achieve higher speed comparisons than the unhardened dynamic bias comparator while gaining SET tolerance at the cost of increased energy per comparison and a small increase in input referred noise.

## V. CONCLUSION

The dynamic bias comparator has been found to be vulnerable to positive and negative SET transients on the biasing structure. Negative transients lead to energy loss, while positive transients degrade preamplifier gain and increase the metastability error rate. A path splitting RHBD technique is effective in mitigating positive SET transients by recovering output voltage by 12.7%, while maintaining the benefits in energy-efficiency and input referred noise. The SET tolerance makes it an improved building block for radiation-hardened ADCs for space applications.

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