A 0.65-pJ/bit 3.6-TB/s/mm I/O Interface with XTalk Minimizing Affine Signaling for Next-Generation HBM with High Interconnect Density

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***Abstract*—This paper presents an I/O interface with Xtalk Minimizing Affine Signaling (XMAS), which is designed to support high-speed data transmission in die-to-die communication over silicon interposers or similar high-density interconnects susceptible to crosstalk. The operating principles of XMAS are elucidated through rigorous analyses, and its advantages over existing signaling are validated through numerical experiments. XMAS not only demonstrates exceptional crosstalk removing capabilities but also exhibits robustness against noise, especially simultaneous switching noise. Fabricated in a 28-nm CMOS process, the prototype XMAS transceiver achieves an edge density of 3.6 TB/s/mm and an energy efficiency of 0.65 pJ/b. Compared to the single-ended signaling, the crosstalk-induced peak-to-peak jitter of the received eye with XMAS is reduced by 75 % at 10 GS/s/pin data rate, and the horizontal eye opening extends to 0.2 UI at a bit error rate $< 10^{-12}$.**

***Index Terms*—High bandwidth memory (HBM), edge density, crosstalk cancellation, simultaneous switching noise, ultra-short-reach (USR) link**

I. Introduction

HIGH-performance computing (HPC) catalyzes transformative developments across diverse domains, encompassing artificial intelligence, cloud computing, natural sciences such as astronomy and physics, and humanities including economics and sociology. In light of its significance, there is a pressing need to enhance HPC's capabilities and address its technological challenges. Nevertheless, as the CMOS technology scaling slows down, the effort for enhancement faces obstacles. Acknowledging these challenges, the emergence of advanced packaging technologies offers promising avenues to sustain technological progress and prolong Moore's Law [1].

High Bandwidth Memory (HBM), where data between a host and memory are transmitted over thousands of silicon interposer channels, can offer high bandwidth suitable for HPC applications, but the demands for even higher bandwidth are rapidly growing to support emerging applications. To maintain overall power budget, higher bandwidth demand should be accompanied by I/O energy efficiency scaling in HBM. Pursuing high bandwidth with low area and energy consumption of the I/O interface leads to the adoption of single-ended (SE) signaling, which exhibits $2\times$ higher pin efficiency than differential signaling for data transmission, over unterminated channels [2], [3]. However, SE brings several disadvantages, particularly its vulnerability to various noise. In systems like HBM having extremely large number of I/O's, the signal deterioration due to data-dependent simultaneous switching noise (SSN) becomes especially pronounced. Various strategies have been explored and developed to mitigate these challenges [4]–[11].

Another key obstacle to higher bandwidth is the crosstalk (XTalk) between the channels. Higher edge density requires small spacing between the channels, increasing crosstalk between neighboring channels [12], [13], which becomes a major threat to signal integrity. To meet the ever-growing demand for higher bandwidth, we should maximize throughput and ensure robustness against noise and crosstalk, while not sacrificing pin efficiency. Addressing this pivotal question forms the core objective of this paper, introducing XTalk Minimizing Affine Signaling (XMAS) as a novel solution to this multifaceted challenge.

Our approach begins with a comprehensive mathematical modeling of XMAS to capture the system performance such as eye width and eye height at the receiver in the presence of crosstalk. This modeling allows design space exploration and strategic co-optimization of the channel and XMAS design to achieve the highest edge density without compromising signaling integrity.

Compared to prior art employing coding or circuit-level techniques for crosstalk cancellation (XTC), the proposed XMAS shows better performance as follows. Conventional bus encoding techniques [14]–[17] add redundant bits to reduce crosstalk, which significantly compromises pin efficiency. Furthermore, as it inherently adopts SE signaling, it is susceptible to noise, making it less robust in systems like HBM. Another prevalent approach involves direct compensation of distortion caused by crosstalk using equalizers [18]–[25]. Despite its effectiveness, this method introduces significant hardware complexity and overhead, worsening the overall I/O energy efficiency. Unlike these methods, XMAS assigns optimized correlation across multiple wires, achieving a remarkable pin efficiency of 87.5 %. Moreover, XMAS ensures robustness against noise and crosstalk without incurring circuit overhead. This novel approach not only addresses the limitations of the previous methods but also offers a balance between pin efficiency and robustness against noise and crosstalk.

This work was supported by the Samsung Electronics Company, Ltd., Hwaseong, Korea.

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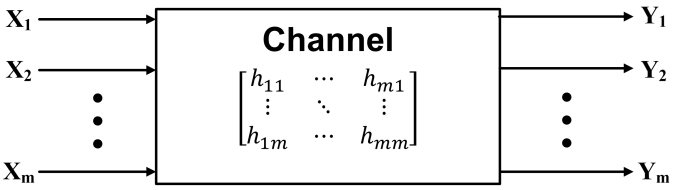


Fig. 1. Multi-input multi-output linear time invariant channel.

The remainder of this paper is organized as follows. Section II presents a mathematical model for XMAS, which serves as the foundation for the co-optimization techniques with the channel detailed in Section III. Section IV introduces the XMAS transmitter and receiver implementations, and Section V presents the measurement results of the prototype transceiver, followed by a conclusion of this work in Section VI.

II. Mathematical Modeling

In XMAS, the transmitter (TX) transmits voltage levels after applying an affine transformation to the incoming parallel binary data, and the receiver (RX) recovers the binary data by linearly transforming the received voltage levels. In the following, we present an analytical model for XMAS that enables cooptimization of signaling and interconnect design presented in Section III.

A. Channel Modeling

Parallel channels with crosstalk can be considered a multi-input multi-output (MIMO) linear time-invariant (LTI) system, which can be described using a set of channel impulse response as shown in Fig. 1. (h_{ij} denotes the channel output Y_j when the input X_i is given as an impulse.) Specifically, when the channel receives the pulse-amplitude-modulated signals, i.e., $X_l(t) = \sum_{i=-\infty}^{\infty} a_{l,i}\Pi(t - iT)$ where $\Pi(t)$ is 1 for $0 \le t < T$ and 0 otherwise, the output can be represented as follows.

$$Y_j = \sum_{i=1}^{m} X_i(t) * h_{ij}(t) = \sum_{i=1}^{m} \sum_{k=-\infty}^{\infty} a_{i,k} E_{ij}(t - kT). \quad (1)$$

$E_{ij}(t)$ denotes the response of the j-th channel to a single-bit-pulse input originating from the i-th channel. If the channel loss is sufficiently small (i.e., intersymbol interference is negligible), the k-th output of j-th channel depends only on the k-th m-parallel inputs $a_{i,k}(i \in [m])$ and $E_{ij}(t)$. For a MIMO channel, we define $\mathbf{H_k}$ as an $m \times m$ matrix whose elements are $E_{ij}(t - kT)$.

B. Encoding/Decoding with Affine/Linear Transformation

In XMAS, an affine transformation is applied to the parallel input data, which are then transmitted by TX using pulse-amplitude modulation. Specifically, an $n \times m$ integer matrix $\mathbf{T}$ is used to encode m-parallel incoming binary data to an n-dimensional integer vector. Then, the encoded elements are

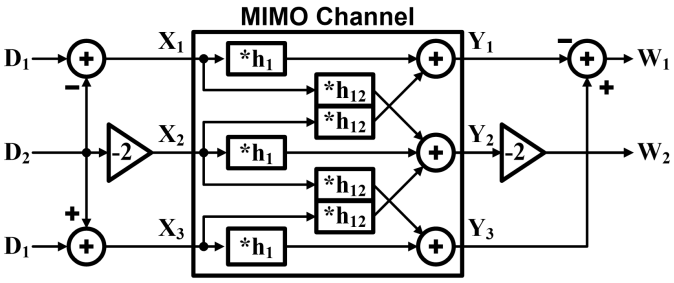


Fig. 2. XMAS example ($n = 3, m = 2$).

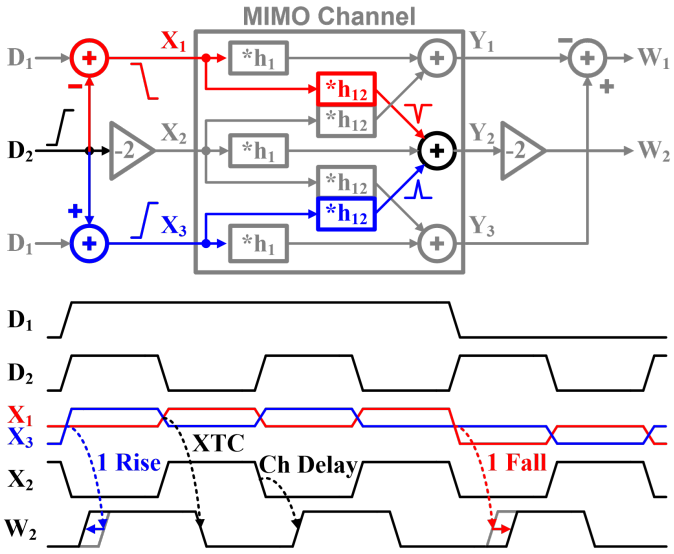


Fig. 3. XTC for W_2.

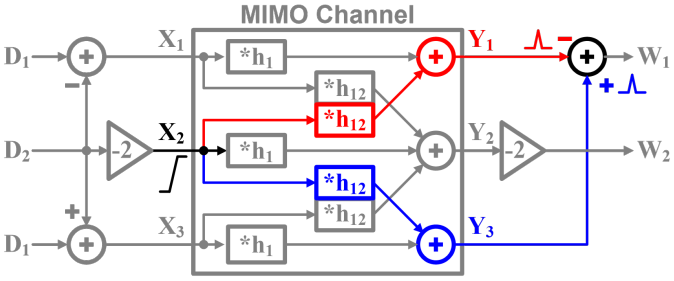


Fig. 4. XTC for W_1.

mapped to the voltage levels $\mathbf{a_i}$ between 0 and V_{DDQ} (supply voltage of the TX output driver), which can be expressed as:

$$\mathbf{a_i} = \left[a_{1,i} \dots a_{n,i}\right]^\intercal = 0.5 \cdot V_{DDQ}(\mathbf{T_{eff}}\mathbf{d_i} + \left[1 \dots 1\right]^\intercal) \quad (2)$$

where $\mathbf{d_i} \in \{-1, 1\}^m$ denotes a vector representing m-parallel binary input to be transmitted, and $\mathbf{T_{eff}}$ is the normalized $\mathbf{T}$ such that the $\ell 1$-norm of each row vector in $\mathbf{T_{eff}}$ becomes 1 to gurarantee that the voltage levels $\mathbf{a_i}$ are within 0 and V_{DDQ}. Then the channel outputs can be represented as $\mathbf{H_i a_i}$, which undergoes a linear transformation at the RX front end. If the linear transformation applied by RX is an $m \times n$ integer matrix

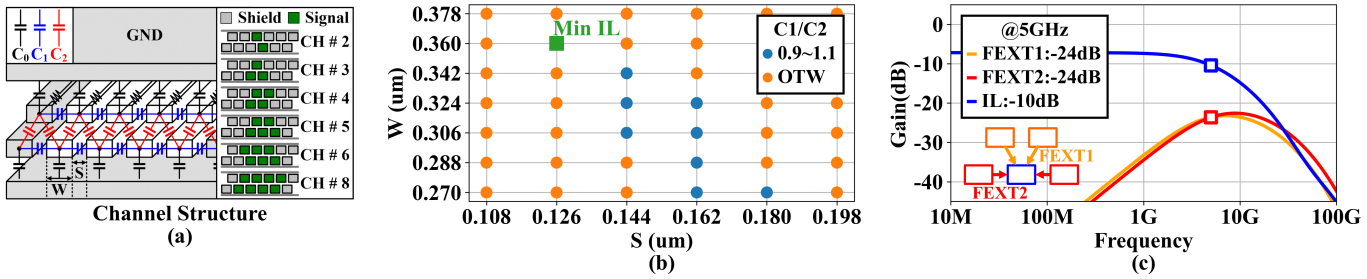


Fig. 5. Channel design parameter (S, W) optimization: (a) Physical structure of channels. (b) Coupling capacitance ratio (C_1/C_2) between adjacent channels as channel width (W) and spacing (S) vary. (c) Channel transfer function with (S, W, L) = (0.126 µm, 0.36 µm, 1.26 mm).

$\mathbf{R}$, then the decoded outputs are[1]

$$\mathbf{W} = \sum_{i=-\infty}^{\infty} \mathbf{R}\mathbf{H_i}\mathbf{a_i} = \sum_{i=-\infty}^{\infty} 0.5V_{DDQ}(\mathbf{R}\mathbf{H_i}\mathbf{T_{eff}}\mathbf{d_i}). \quad (3)$$

As a toy example, Fig. 2 illustrates XMAS with below matrices, where two input data are encoded over three channels.

$$\mathbf{T} = \begin{bmatrix} 1 & -1 \\ 0 & -2 \\ 1 & 1 \end{bmatrix} \quad \mathbf{R} = \begin{bmatrix} -1 & 0 & 1 \\ 0 & -2 & 0 \end{bmatrix}$$

$$\mathbf{H} = \begin{bmatrix} h_1 & h_{12} & 0 \\ h_{12} & h_1 & h_{12} \\ 0 & h_{12} & h_1 \end{bmatrix}$$

Inputs D_1 and D_2 are encoded by $\mathbf{T}$ into a set of signals (X_1, X_2, X_3) transmitted through the channels. The channel characteristics are defined by $\mathbf{H}$, where each channel has identical pulse response h_1, and the symmetric coupling between adjacent channels is denoted by h_{12}. Channel outputs (Y_1, Y_2, Y_3) are then decoded by matrix $\mathbf{R}$ into symbols $W_1 = \hat{D}_1$ and $W_2 = \hat{D}_2$. Due to the channel structure, the channel inputs X_1 and X_3 influence Y_2, causing crosstalk-induced jitter (CIJ). However, as depicted in Fig. 3, the input D_2 is added with the opposite signs into the red and blue paths, effectively canceling the crosstalk at Y_2. In more detail, when input data in Fig. 3 are given, X_1 and X_3 transition in the exactly opposite directions, perfectly canceling out the crosstalk, or when one signal (X_1) undergoes a full swing transition, the transition in the other signal (X_3) is always prevented, thereby reducing CIJ. Another source of crosstalk is the influence of X_2 on Y_1 and Y_3. As shown in Fig. 4, X_2 causes the same amount of distortion in Y_1 and Y_3, which is perfectly canceled during decoding. Such properly designed XMAS matrices thus can hold significant potential for XTC. Hence, in the following, we show how to carefully design the XMAS matrices with the channels to maximize the interface edge density by taking advantage of excellent XTC with XMAS.

III. XMAS Design

This section focuses on determining the XMAS and channel design parameters, aiming to maximize edge density in dense channel environments. Edge density is affected by various design parameters such as channel dimensions, per-pin data rate, and XMAS matrices. The intricate interplay of diverse parameters significantly influences edge density, making it complex and challenging to find optimal parameters achieving the best performance. Moreover, since the number of possible encoding and decoding matrices in XMAS is vast and simulating each case is computationally complex and time-consuming, finding an optimal parameter set without a theoretical model is practically infeasible. Thus, the analytical model described in Section II is leveraged to efficiently navigate the expansive parameter space and to find the optimal parameters for the maximum edge density. Specifically, the optimization problem for the prototype XMAS transceiver is defined as follows:

$$\begin{aligned} \max_{S,W,L,\mathbf{T_{n\times m}},\mathbf{R_{m\times n}},B} \quad & \text{Edge Density} \quad (4) \\ \text{subject to} \quad & \text{Eye Width} \geq 0.7\,\text{UI, Height} \geq 100\,\text{mV} \\ & \text{Channel Loss} \leq 10\,\text{dB, } 0.9 \leq \frac{C_1}{C_2} \leq 1.1 \end{aligned}$$

where S, W, L, C_1, and C_2 denote the channel spacing, width, length, capacitance between the adjacent channels in the same layer and different layers, respectively (see Fig. 5(a)), and B represents the symbol rate (Baud). Note that the last two constraints in (4) are added so the designed channels have low loss and symmetric capacitance between adjacent channels.

A. Codesign of Interconnects with Signaling

Fig. 5(a) depicts the adopted channel layout, following the densely structured approach of [19] to maximize the interconnect density. The number of wires grouped for encoded data transmission, determined by the number of rows (n) in the XMAS encoding matrix $\mathbf{T}$, can be adjusted to alter the channel configuration, and the width (W) and spacing (S) of the channels determine their characteristics such as the channel resistance and capacitance as well as the coupling capacitance between adjacent channels. Fig. 5(b) illustrates the variation of the coupling capacitance ratio C_1/C_2 as W and S change. A ratio close to 1 indicates symmetric crosstalk from adjacent channels, represented as the blue dots in Fig. 5(b)[2]. Among them, the configuration with the lowest insertion loss (IL),

[1]In (3), the bias term due to $[1 \ldots 1]^\intercal$ in (2) is omitted since $\mathbf{R}$ will be chosen to make the bias term become zero.

[2]Although not mandatory, symmetric crosstalk yields simpler XMAS design, so the ratio close to 1 is chosen for the prototype implementation.

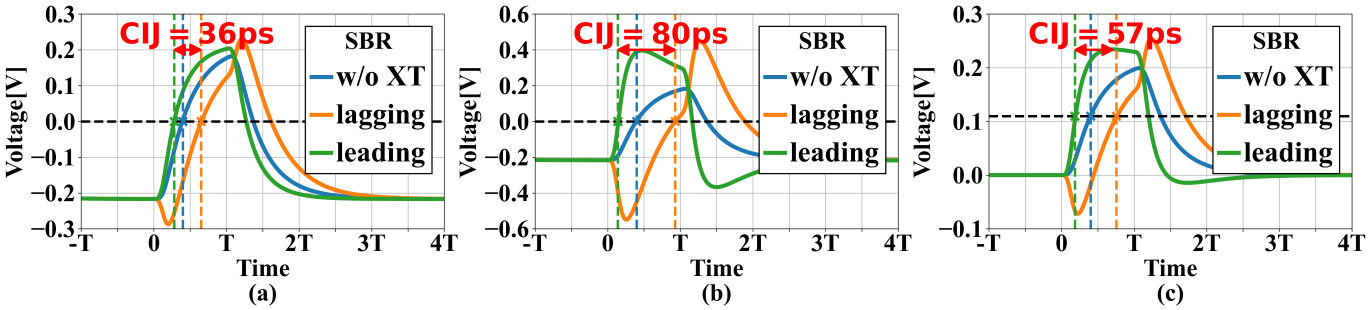


Fig. 6. Impact of crosstalk-induced jitter on SBR: (a) XMAS with optimized matrices. (b) XMAS with degenerate matrices. (c) Single-ended signaling.

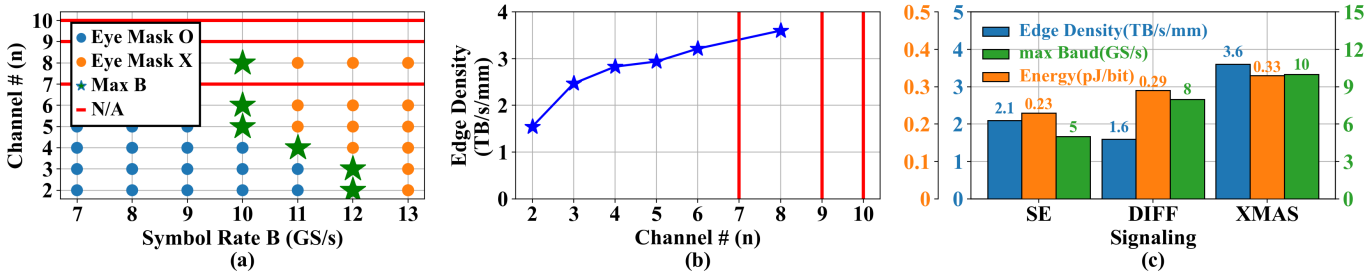


Fig. 7. XMAS parameter optimization (n, m, B): (a) Representing whether required eye mask is satisfied or not as symbol rate (B) and number of channels (n) vary. (b) Maximum achievable edge density for different number of channels. (c) Comparison of edge density, maximum symbol rate, and energy efficiency between different signaling schemes.

R

4	-4	0	0	0	0	0	0
0	0	-4	4	0	0	0	0
-2	-2	2	2	0	0	0	0
0	0	0	0	-4	4	0	0
0	0	0	0	0	0	-4	4
0	0	0	0	-2	-2	2	2
-1	-1	-1	-1	1	1	1	1

T

4	0	-3	0	0	0	-2
-4	0	-3	0	0	0	-2
0	-4	3	0	0	0	-2
0	4	3	0	0	0	-2
0	0	0	-4	0	-3	2
0	0	0	4	0	-3	2
0	0	0	0	-4	3	2
0	0	0	0	4	3	2

Fig. 8. Proposed XMAS matrices.

which corresponds to $S = 0.126\,\mu\text{m}$ and $W = 0.36\,\mu\text{m}$, is marked with the green square and chosen for the prototype. When the eight wires are designed with $(S, W, L) = (0.126\,\mu\text{m}, 0.36\,\mu\text{m}, 1.26\,\text{mm})$, the channel characteristics are obtained as Fig. 5(c). At a frequency of 5 GHz, the insertion loss is around 10 dB, and the far-end crosstalk (FEXT) reaches -24 dB, primarily emanating from the four adjacent channels. These channels emerge as the principal sources of interference, whereas more distant channels have a negligible impact on the overall crosstalk.

B. XMAS Matrix Design

For the described channel configuration, the XMAS matrices $\mathbf{T}$ and $\mathbf{R}$ are designed to possess the following properties that significantly improve signal integrity.

1) Binary Decision: Although pulse-amplitude-modulated signals are transmitted through channels, RX makes a binary decision with XMAS, which minimizes the sensitivity to intersymbol interference due to channel loss, similar to chord signaling [10]. To this end, the XMAS encoding and decoding matrices, $\mathbf{T}$ and $\mathbf{R}$, are designed such that every row vector in $\mathbf{R}$ and every column vector in $\mathbf{T}$ are orthogonal. In other words, for some diagonal matrix $\mathbf{\Lambda}$,

$$\mathbf{RT} = \mathbf{\Lambda}. \tag{5}$$

With this condition, due to (3), the decoded outputs will have binary levels.

2) Minimal Crosstalk-Induced Jitter (CIJ): For the designed channels, Fig. 6 shows the simulation result demonstrating the impact of CIJ on single-bit response (SBR), where the zero-crossing times are either delayed or advanced depending on the data pattern. This distorted SBR can be accurately captured by substituting appropriate patterns into $\mathbf{d_i}$ as each element of $\mathbf{W}$ in (3) represents the output waveform at the RX. For instance, CIJ-induced SBR for the channel #4 (W_4) can be calculated by evaluating (3) after setting $\mathbf{d_i}$ such that a single bit pulse is given to d_4 (i.e., $d_{i,4} = 1$ and $d_{j,4} = -1$ for $j \neq i$), and all the possible combinations of data patterns are provided to the other data. Then, CIJ_4, which is the largest difference between the zero-crossing times for W_4, can be readily calculated based on the computed SBRs. Note that, since the SBR waveforms are determined by $\mathbf{T}$ and $\mathbf{R}$, proper matrix selection for given channels ($\mathbf{H_i}$) helps minimize CIJ. As illustrated in Fig. 6, with the optimal selection of $\mathbf{T}$ and $\mathbf{R}$, CIJ can be greatly reduced; otherwise, CIJ can become worse than SE.

3) Minimal SSN: The encoding matrix in XMAS is constructed so the set of voltage levels formed by the n TX drivers can be always constant, i.e., each driver may transmit different voltage during each unit interval (UI), but as a group

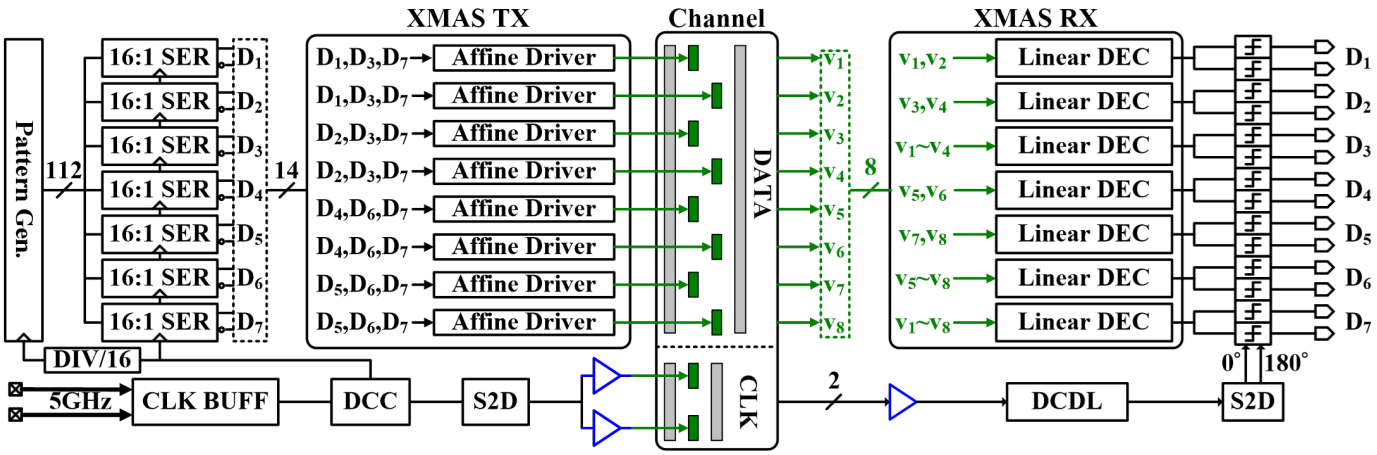


Fig. 9. Overall architecture of the proposed transceiver with XMAS.

of n drivers, they always transmit the identical voltages. For instance, for the 7×8 encoding matrix $\mathbf{T}$ presented in Fig. 8, eight voltages of $V_{DDQ} \cdot [0, 2/9, 3/9, 4/9, 5/9, 6/9, 7/9, 1]$ are invariably used by eight drivers. In other words, regardless of seven input data, the eight encoded data have one of the values in $V_{DDQ} \cdot [0, 2/9, 3/9, 4/9, 5/9, 6/9, 7/9, 1]$, and each driver transmits distinct voltage levels. This ensures that the current provided from the supply to the drivers remains constant irrespective of input data, thereby greatly removing SSN.

Having discussed the desired XMAS properties, now we describe how to design $\mathbf{T}$ and $\mathbf{R}$ for XMAS. Once the channel dimensions S, W, and L are determined, for the fixed values of m and n, integer matrices $\mathbf{T}$ and $\mathbf{R}$ can be determined to satisfy the required properties. To improve pin efficiency and maximize edge density, the number of parallel data to be encoded (m) is fixed at $n - 1$. Fig. 7(a) depicts the symbol rates (B) that satisfy the eye mask constraints in (4), with each set of optimized matrices $\mathbf{T}$ and $\mathbf{R}$ uniquely determined for the fixed channel configuration across various values of n. Note that, for n equal to 7 or greater than 8, the orthogonality condition (5) is unattainable, which is illustrated by a red line in Fig. 7(a). As n decreases, the maximum symbol rate meeting the eye mask constraint tends to increase, suggesting that a smaller n yields better XTC performance of XMAS. However, this also results in lower pin efficiency, thereby not necessarily yielding the highest edge density. Fig. 7(b) illustrates the edge density at the maximum symbol rate for each n value. While the XTC performance of XMAS may decrease as n increases, higher pin efficiency leads to an increase in edge density. Consequently, for maximum edge density, we choose n = 8 and the corresponding optimal orthogonal matrices $\mathbf{T}$ and $\mathbf{R}$ are depicted in Fig. 8. For the identical channel configuration and eye-opening conditions, XMAS outperforms SE and differential signaling thanks to its high XTC performance even at a maximum symbol rate of 10 GS/s. Moreover, its high pin efficiency (7/8) allows XMAS to achieve 1.7× and 2.25× higher edge density compared with SE and differential signaling, respectively, while maintaining comparable energy efficiency, as illustrated in Fig. 7(c).

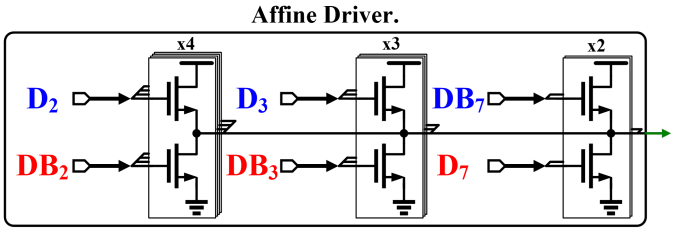


Fig. 10. Affine driver implementation corresponding to the row vector [0 4 3 0 0 0 -2].

IV. XMAS Interface Architecture

Fig. 9 illustrates the overall architecture of the proposed interface with XMAS. TX serializes the 16×7 bits of parallel data by 16:1 serializers (SERs) and supplies 7 parallel differential data stream to the 8 affine drivers, which drive the channels with appropriate voltages. The affine drivers encode the parallel incoming data following the row vectors of $\mathbf{T}$ in Fig. 8. Since each row of $\mathbf{T}$ consists of three non-zero elements, each driver takes three out of seven parallel incoming data as shown in Fig. 9. At the RX front end, the linear decoders, implemented following the row vectors of $\mathbf{R}$, convert the received voltages from 8 channels into 7 binary symbols to restore the data. For the clock path, a limited-swing half-rate differential clock is forwarded to the RX, amplified by a CML-to-CMOS converter [26], and a digitally-controlled delay line (DCDL) [27] is used to compensate for the skew between data and clock.

The TX affine driver consists of multiple N-over-N drivers, where each row vector of $\mathbf{T}$ determines the weight of each driver. For instance, as illustrated in Fig. 10, the driver corresponding to the row vector [0 4 3 0 0 0 -2] consists of N-over-N drivers with weights of 4, 3, and 2, respectively. Pull-up inputs for each driver are D_2, D_3, and $\bar{D}_7$, and pull-down inputs are $\bar{D}_2$, $\bar{D}_3$, and D_7. This implementation generates the output voltage level of $V_{CM} + V_R(4D_2 + 3D_3 - 2D_7)$, which is an affine transformation of (D_2, D_3, D_7). Supply voltage of the driver in the prototype is chosen to be 0.4 V to minimize power. Fig. 11 illustrates the device-mismatch-

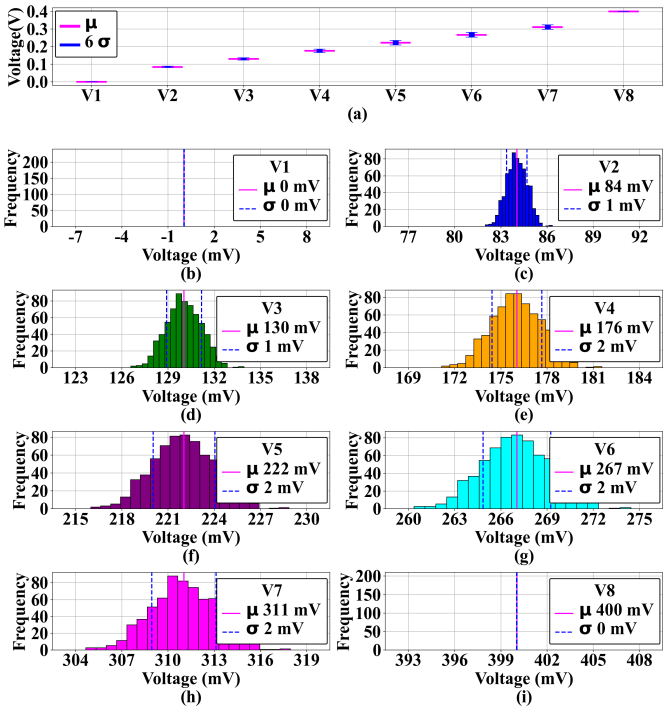


Fig. 11. Simulated affine driver output voltage variation.

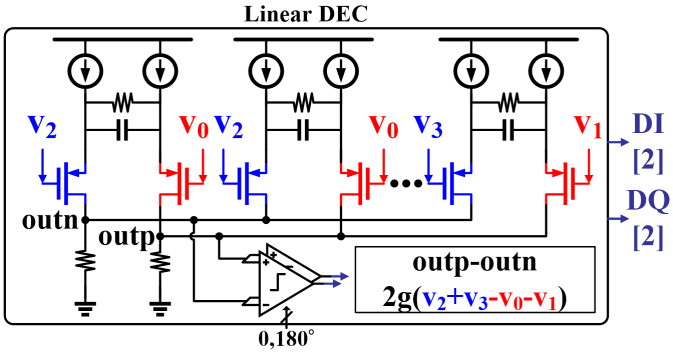


Fig. 12. Linear decoder implementation corresponding to the row vector [-2 -2 2 2 0 0 0 0].

induced distribution of 8 analog voltage levels produced by the designed affine driver. It also presents the histograms of voltage distributions for each output level, which demonstrates that the output voltage level variation due to device mismatch is negligible.

Similar to the TX, the RX decoders at the front end are implemented, following the row vectors of $\mathbf{R}$, to restore the binary symbol through a linear transformation. For instance, Fig. 12 shows the decoder implementation corresponding to the row vector [-2 -2 2 2 0 0 0 0] in $\mathbf{R}$. Differential pairs with capacitive source degeneration allows RX to compensate for channel loss and to perform $v_3 - v_1 + v_4 - v_2$ operation with some gain for recovering D_3. All the seven decoders employ the identical topology with the appropriately chosen channel inputs based on $\mathbf{R}$.

We validate the effectiveness of the proposed XMAS interface through simulation results. As shown in Fig. 13(a,b), compared to SE, thanks to its XTC performance XMAS reduces CIJ from 55 ps to 30 ps. This timing margin improvement becomes even more pronounced in the presence of SSN. With a supply inductance of 5 nH, as shown in Fig. 13(c,d), while the SE eye completely closes, the XMAS eye is not degraded at all. In case of SE, even with small supply inductance, SE experiences huge peak-to-peak jitter caused by both SSN and CIJ, which leads to significantly degraded signal integrity especially at higher data rates (see Fig. 14(b)). On the other hand, XMAS does not suffer from SSN at all, and as shown in Fig. 14(a), XMAS consistently demonstrates around 45 % jitter reduction on average across various symbol rates compared to SE even in SSN-free environments.

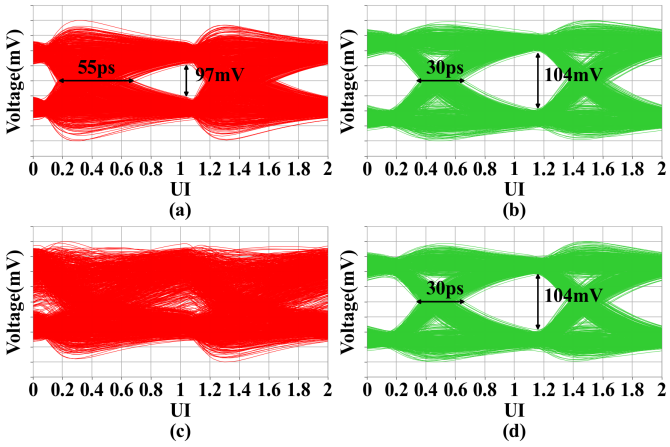


Fig. 13. RX eye diagrams: (a) SE without SSN, (b) XMAS without SSN, (c) SE with SSN, and (d) XMAS with SSN (5 nH supply inductance).

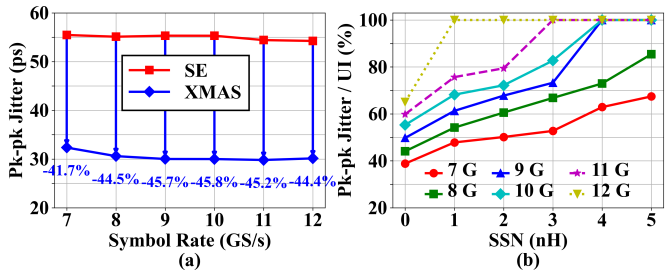


Fig. 14. (a) Peak-to-peak jitter reduction with XMAS across various symbol rates. (b) Peak-to-peak jitter with SE for various supply inductances and data rates.

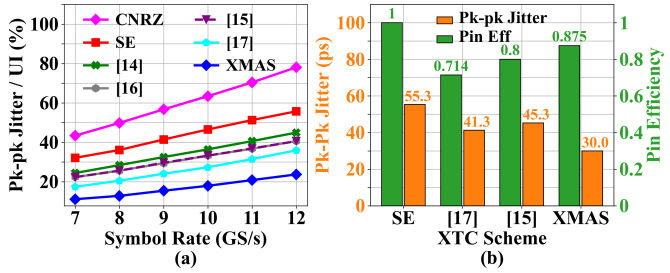
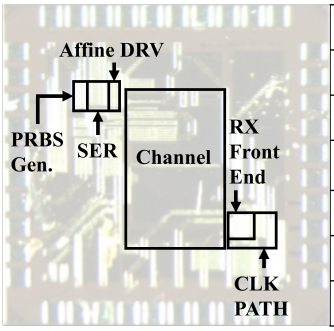


Fig. 15. (a) CIJ for various bus encoding techniques across different data rates. (b) Performance comparison of bus encoding techniques and XMAS.

Prior bus coding techniques typically encode the data to



@ 70Gbps	Power(mW)	Area(mm²)
Serializer	14.24(32%)	0.0034(46%)
Affine DRV	12.88(29%)	0.0003(4%)
RX Front End	8.28(19%)	0.0018(24%)
CLK PATH	8.15(18%)	0.0017(23%)
Others	0.98(2%)	0.0002(3%)
Total	44.53	0.0074

Fig. 16. Chip photomicrograph and power breakdown.

avoid transmitting symbols sensitive to crosstalk by adding redundant bits, which limits the achievable pin efficiency. Comparison between prior art and XMAS is depicted in Fig. 15. For a fair comparison, all methods are compared at a fixed pin efficiency of 75 %[3] with the identical channels. Among prior art, [17] achieves the highest XTC performance but uses a differential code, and [14] employs Fibonacci coding for XTC, where the encoders add logical distance between symbols. These works use digital logic to perform encoding/decoding, which incurs a long end-to-end latency. On the other hand, since XMAS encodes/decodes the data without any digital logic, it does not incur any coding latency, while providing superior XTC performance. In the case of chord signaling [10], the XTC performance can vary significantly and may even boost the crosstalk depending on the MIMO channel characteristics. In other words, chord signaling [10] does not necessarily guarantee XTC performance. Fig. 15(b) compares the pin efficiency and peak-to-peak jitter of XMAS with those of prior art with the highest XTC performance. In conclusion, XMAS shows the highest pin efficiency, while achieving the lowest CIJ without incurring additional coding latency.

V. Measurement Results

The prototype transceiver was fabricated in a 28 nm CMOS technology. Fig. 16 shows the die photo and the power breakdown of the chip. 7-bit-parallel data are encoded and transmitted at 10 GS/s/pin through eight channels (i.e., 70 Gb/s aggregate bandwidth). The overall transceiver occupies an active area of 0.0074 mm^2 and consumes 44.53 mW.

Fig. 17 shows the measured bathtub curves of XMAS and SE at 10 Gb/s. As shown in Fig. 17(a), the proposed XMAS allows all seven data to have a timing margin at least 0.2 UI at a BER of 10^{-12}. Since the test chip does not have any per-pin deskew circuit, D_7 has a timing skew of about 0.175 UI, but the proposed XMAS achieves error-free operation for all the data. However, the timing margin with SE is severely degraded with crosstalk, and BER lower than 10^{-5} cannot be achieved with four aggressors (see Fig. 17(b)). The voltage margin is also significantly improved with XMAS as demonstrated in Fig. 18. For SE, the eye width and height

[3]The XMAS matrices are modified to transmit 3 data over 4 channels for comparison.

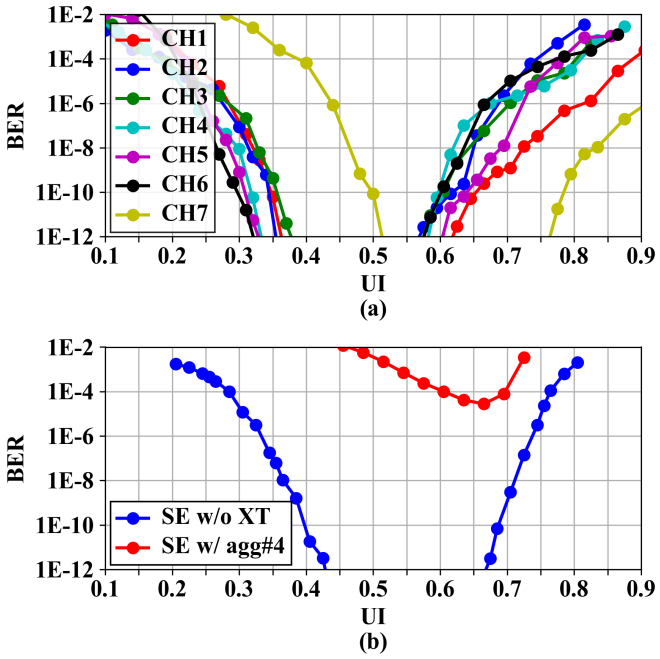


Fig. 17. Measured bathtub curves at 10 Gb/s: (a) XMAS tested with PRBS15, and (b) SE tested with PRBS7.

decrease rapidly as the number of aggressors increases. Even with three aggressors, SE cannot achieve BER less than 10^{-9}, while XMAS has a margin of 0.24 UI width and 32 mV height with four aggressors. XMAS provides larger voltage and timing margin compared to SE with just one aggressor (see Fig. 18(f)). Peak-to-peak jitter for SE without any crosstalk is measured to be 68 ps, and Fig. 18(f) shows that SE suffers from CIJ even with one aggressor, increasing jitter to 82 ps, while XMAS is capable of greatly suppressing CIJ and jitter is only 76 ps with four aggressors.

Compared with other state-of-the-art XTC schemes, XMAS shows the best XTC performance and achieves the highest edge density with comparable energy efficiency and area. One popular XTC method [20] uses circuit-level techniques, where the receiver integrates a continuous-time compensation equalizer with a decision feedback equalizer (DFE). The DFE is further augmented with logic that removes post-taps due to crosstalk. However, this approach suffers from significant power and area overhead due to its complex equalizer configuration. Another method [28] mitigates crosstalk by dividing the transmission bandwidth and splitting the phase in high-frequency bands. Though different from adjusting transmission delay for XTC [29], it shares similarities with phase domain equalization as it separates noise sources in the phase domain and applies to the filter. Coding-based XTC schemes, on the other hand, eliminates the need for complex equalizers and exhibit good area and power efficiency, but they generally face limitations such as low pin efficiency and large coding latency.

Fig. 19(a) illustrates the area, energy, and pin efficiency of various XTC schemes, where XMAS, despite being coding-based, shows almost the best energy efficiency and minimal hardware overhead with pin efficiency close to 1. Additionally,

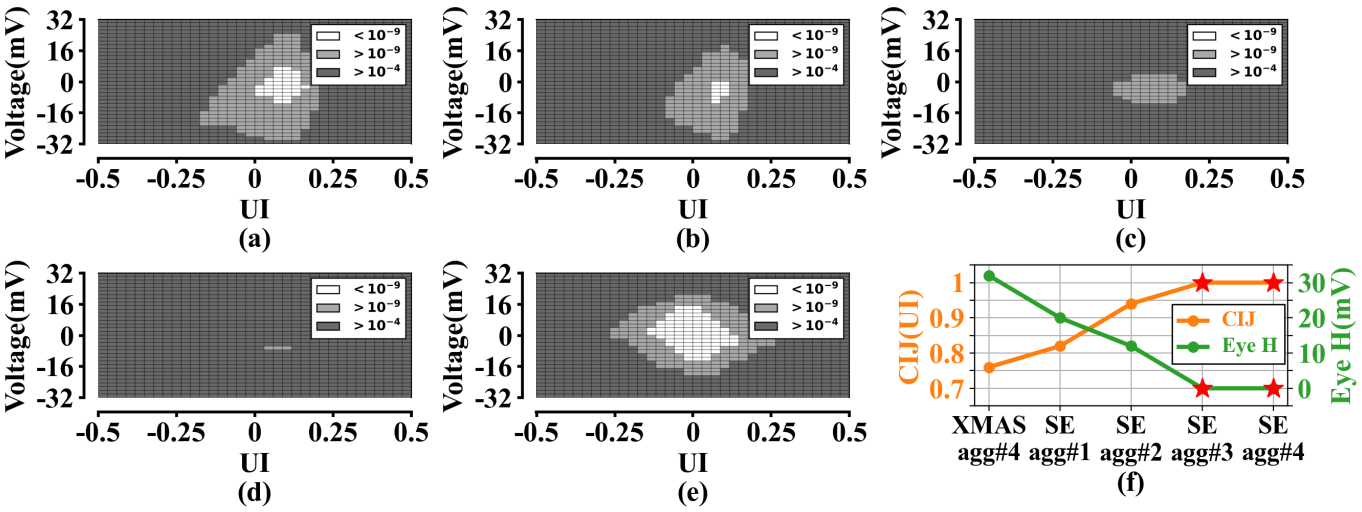


Fig. 18. Measured eye diagrams: (a) SE with 1 aggressor, (b) SE with 2 aggressors, (c) SE with 3 aggressors, (d) SE with 4 aggressors, (e) XMAS with 4 aggressors, and (f) eye height and peak-to-peak jitter across for different cases (BER at 10^{-9}).

TABLE I
COMPARISON WITH STATE-OF-THE-ART XTC SCHEMES AND ON-CHIP INTERFACES.

	[20]	[28]	[19]	[25]	[14]	[32]	This work
Technology	32 nm	28 nm	65 nm	28 nm	28nm	5 nm	28 nm
Signaling	SE	SE	SE	SE	SE	SE	XMAS
Data Rate/pin (Gb/s)	7	6	4	28	10	25.2	10
Pin Efficiency(%)	100	100	100	100	75	100	87.5
Edge Density (TB/s/mm)	0.0032	N/A	0.75	N/A	0.0354	0.725	3.6
XTC scheme	CTXC+DFXC	PXC	FFE	CTXC	Coding	N/A	Coding
FEXT@Nyquist(dB)	-29.5	-12	-31.8	+12	-7.8	-42.2	-24
Jitter Reduction	N/A	N/A	78%	N/A	45%	N/A	75 %
Eye Opening (BER)	0.13 UI (10^{-12})	0.2UI (10^{-12})	0.4UI (10^{-9})	0.3UI (10^{-12})	0.58UI (10^{-12})	0.66UI (10^{-12})	0.2UI (10^{-12})
Area (mm^2/lane)	0.012	0.004	0.008	0.035	0.004	0.0042	0.001
Energy Efficiency (pJ/bit)	8 (RX)	0.6 (RX)	1.5 (TX+RX)	0.85 (RX)	1.29 (TX+RX)	0.19 (TX+RX)	0.65 (TX+RX)

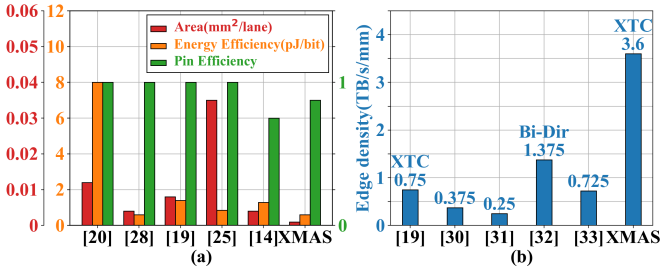


Fig. 19. Performance comparison: (a) area, power and pin efficiency with other XTC schemes, and (b) edge density with recent on-chip interfaces.

XMAS achieves the highest edge density compared to the studies over the past three years (see Fig. 19(b)) [19], [30]–[33]). Table I compares state-of-the-art interfaces over the past five years. Notably, the XMAS transceiver excels by achieving a great edge density of 3.6 TB/s/mm, an energy efficiency of 0.65 pJ/bit, and an area efficiency of 0.0012 mm^2/lane.

VI. CONCLUSION

This paper introduces an I/O interface with the novel signaling XMAS, which is designed to support high-speed data transmission over channels with high crosstalk. XMAS not only demonstrates exceptional crosstalk removing capabilities but also exhibits robustness against noise, especially simultaneous switching noise. To maximize the edge density, co-optimizing the design of channels and signaling is performed using an analytical model of XMAS. The prototype XMAS transceiver is fabricated in a 28-nm CMOS process and achieves an edge density of 3.6 TB/s/mm with an energy efficiency of 0.65 pJ/b. Compared to SE, CIJ of the received eye with XMAS is reduced by 75 % at 10 GS/s/pin data rate, and the horizontal eye opening extends to 0.2 UI at a bit error rate less than 10^{-12}.

ACKNOWLEDGMENTS

The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

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